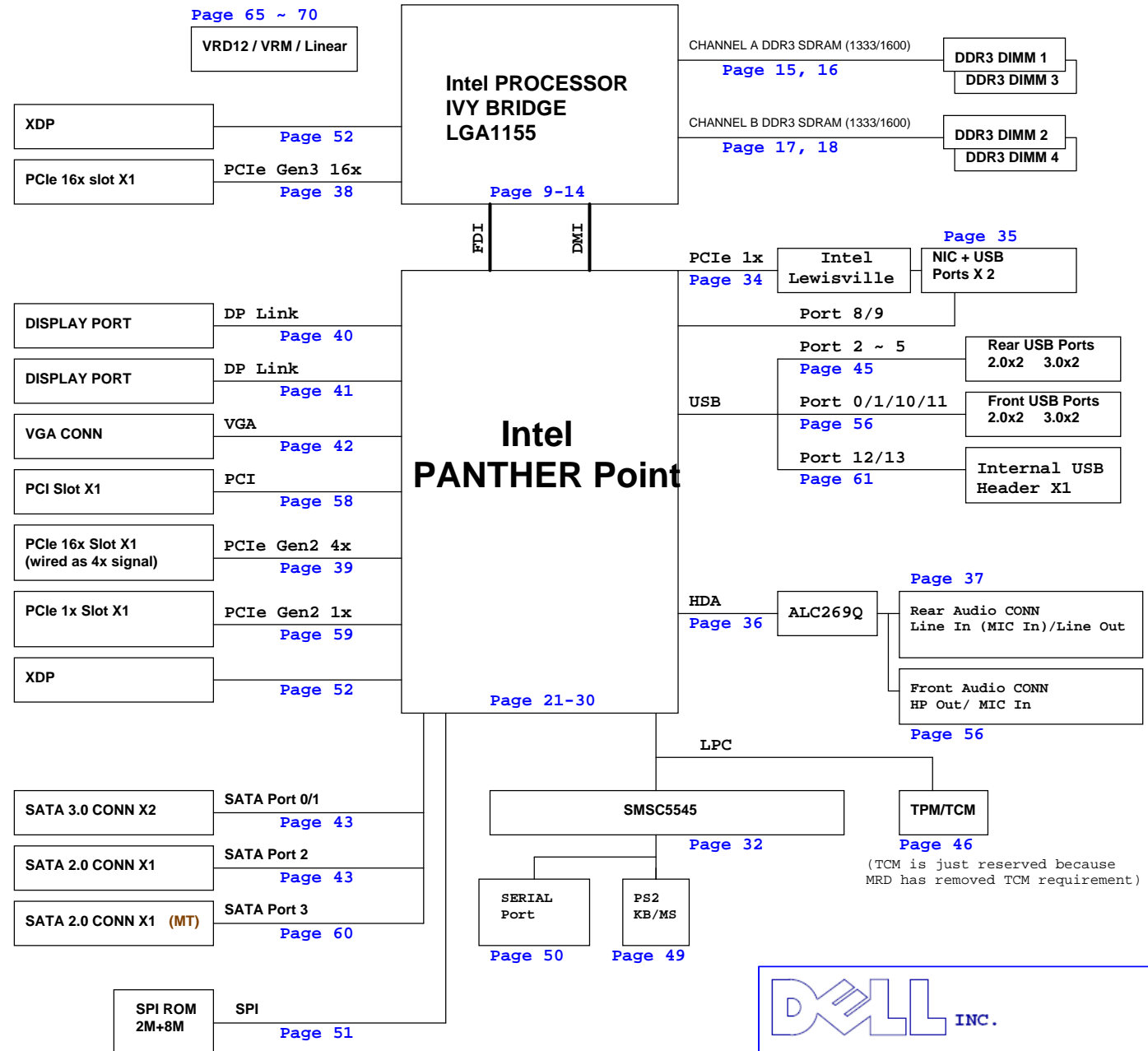



Lainikai - MT / DT

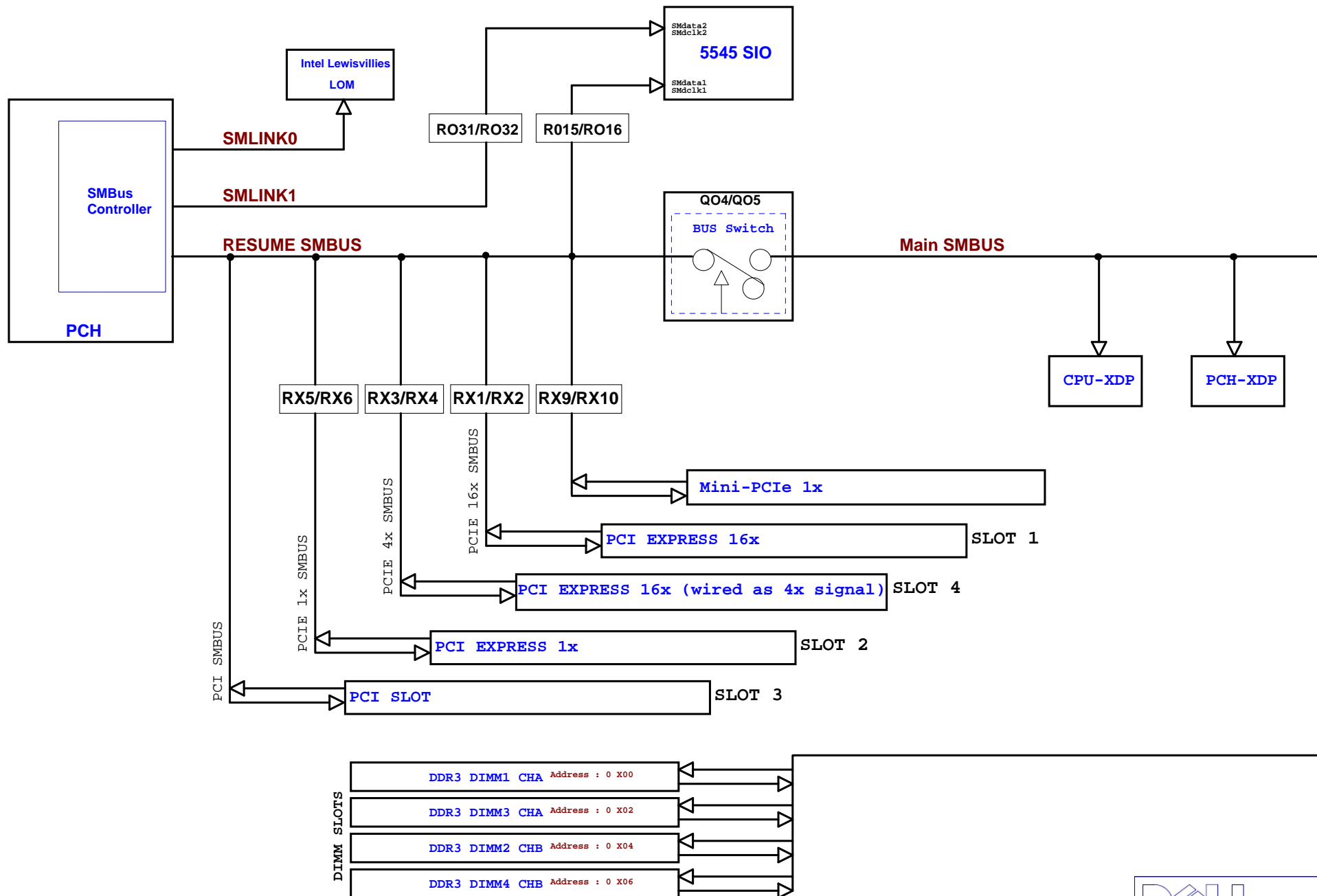
1. Index / Block diagram
2. SMBus MAP
3. Clock Distribution
4. Power Delivery Map
5. Power On Sequence
6. Reset / Power Good Map
7. Strap/IRQ/IDSel Table
8. GPIO Table
- 9-14. CPU
- 15-16. DDR3 Conn: CHA
- 17-18. DDR3 Conn: CHB
19. TBD
20. TBD
- 21-30. PCH
31. PCH MISC Conn/BUZ/ID
- 32-33. SIO:SMSC5544
- 34-35. LAN: INTEL LEWISVILLE
- 36-37 AUDIO:ALC269Q
38. Slot1: PCIe 16x
39. Slot4: PCIe 4x
40. Display Port 1
41. Display Port 2
42. VGA Conn
43. SATA Conn
44. TBD
45. Rear USB
46. TPM & TCM
47. Thermal Sensor Conn
48. FAN
49. PS2 Conn
50. COM1
51. SPI
52. XDP
53. Pilot Run Conn
54. EMI
55. COM2 HDR
56. Front Panel
57. Front USB 3.0
58. Slot3: PCI
59. Slot2: PCIe 1x
60. SATA_MT
61. Flexbay USB
62. TBD
63. Power Conn
64. Power Sequence
- 65-66. Power: Linear Power
- 67-68. Power: Vcore PWM
- 69-70. Power: VCCIO/VCCSA
71. Power: DDR3/5Vdual/5VUSB

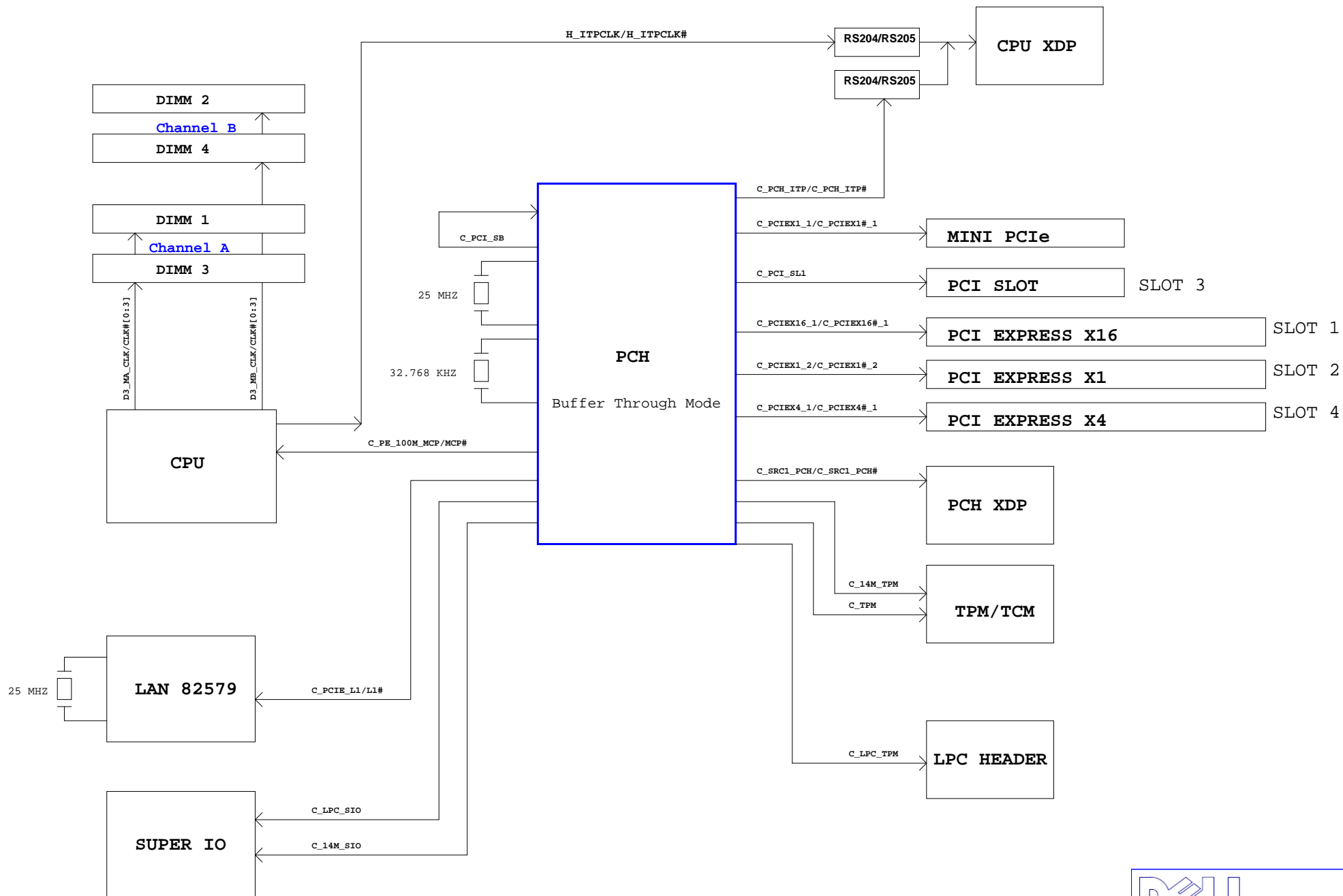


DESIGN	CHECK	APPROVE
Hiko	Hiko	Ivan

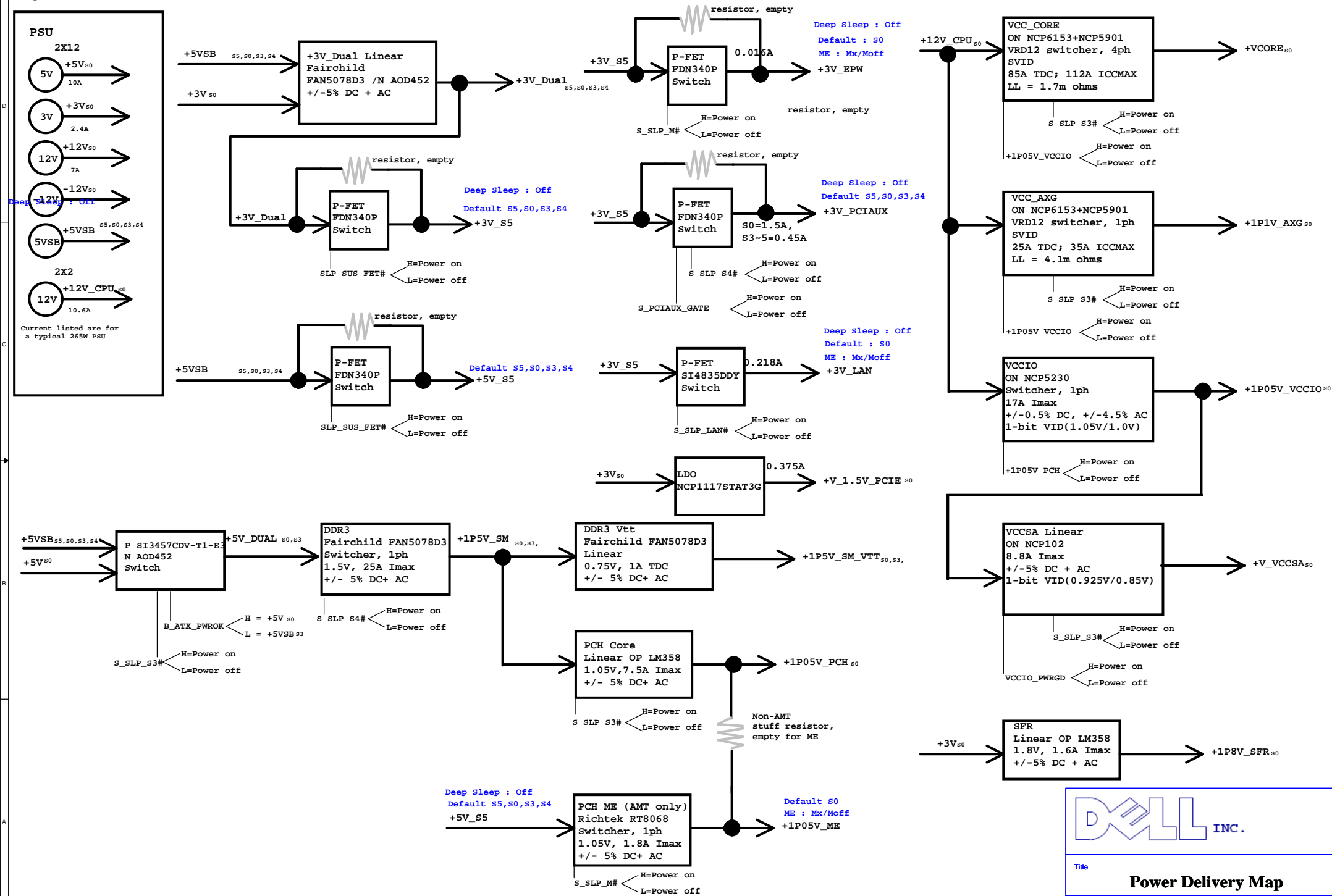
		
Title		
Index / Block diagram		
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SMBUS DIAGRAM





POWER DELIVERY MAP



Title

Power Delivery Map

DWG NO	
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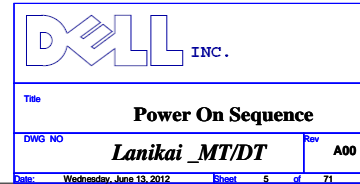
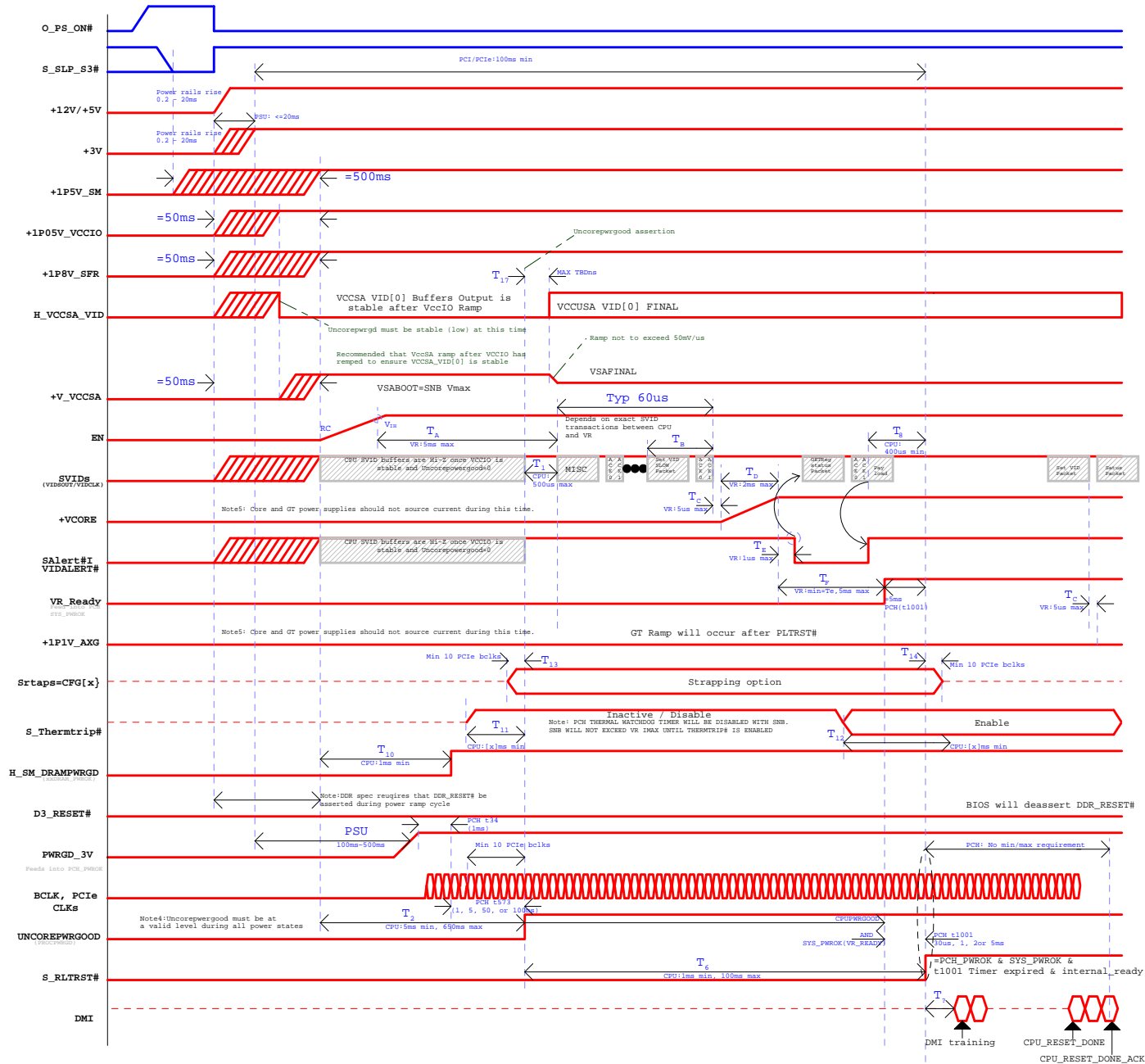
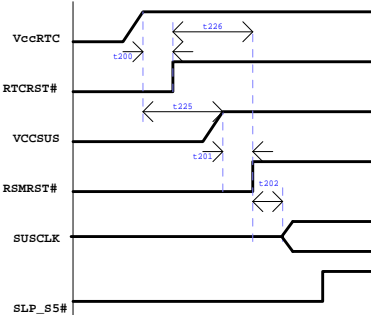
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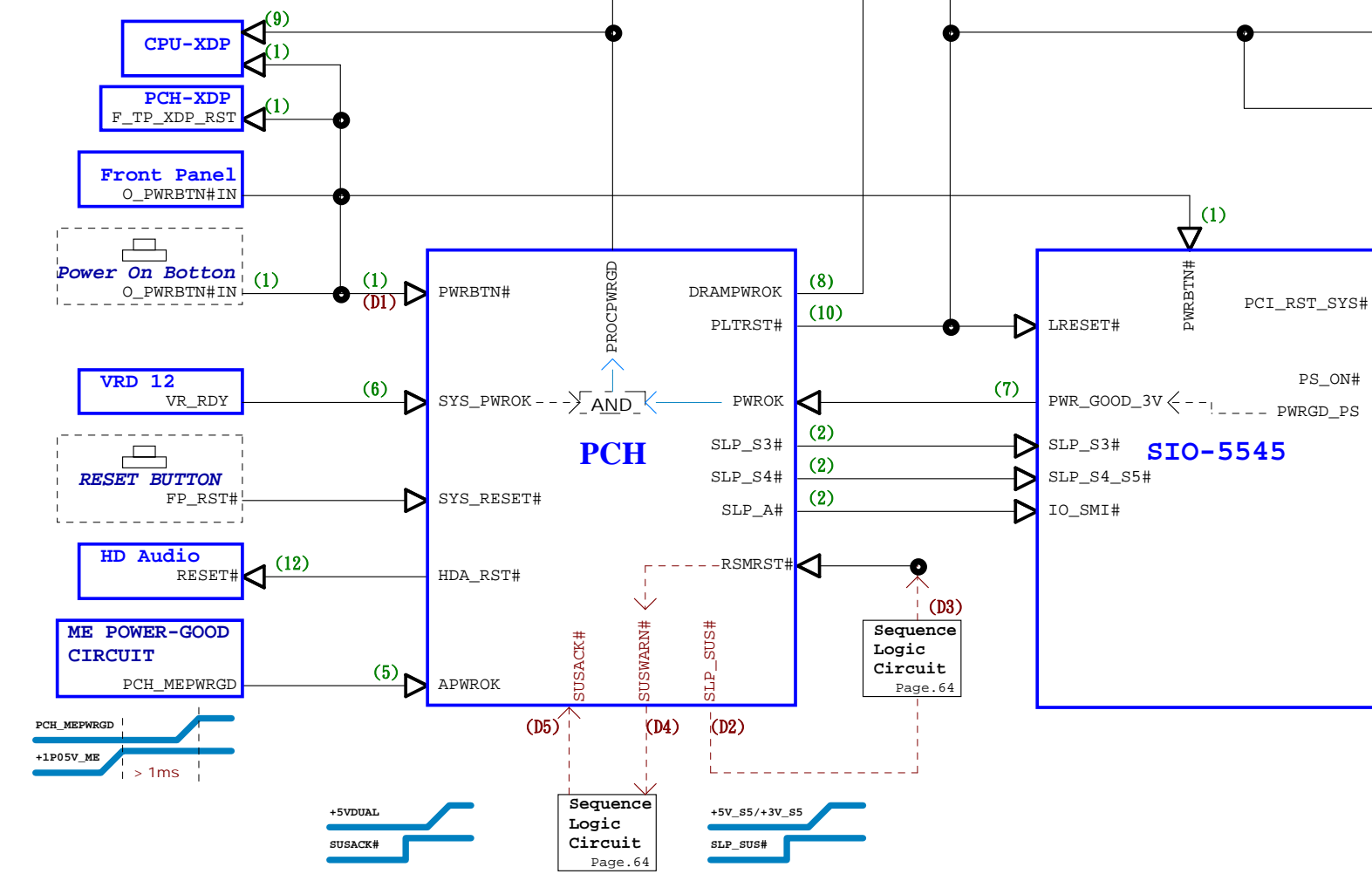
G3 to S4/S5 Timing Diagram



RESET / Power Good MAP

Sequence Signal Name:

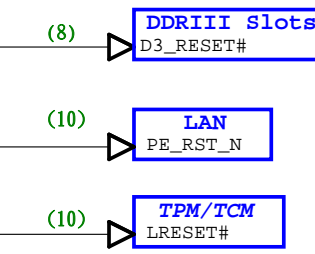
- (1) O_PWRBTN#IN
- (2) S_SLP_S4# S_SLP_S3# S_SLP_M#
- (3) O_PSON#
- (4) B_ATX_PWROK
- (5) PCH_MEPWRGD
- (6) S_PCH_SYSPWROK P_VR_READY
- (7) PWRGD_3V
- (8) H_DRAMPWROK D3_RESET#
- (9) H_PWRGD
- (10) S_PLTRST# H_RESET#_R S_PLTRST#_R
- (11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
- (12) A_Z_RST#



Deep Sleep Exit MAP

Sequence Signal Name:

- (D1) O_PWRBTN#IN
- (D2) S_SLP_SUS#
- (D3) S_RSMRST#
- (D4) S_SUSWARN#
- (D5) S_SUS_PWR_ACK#



IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot3	C	D	A	B	18	0	0

STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	C_CK505_33M_PCI2	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI4/SRC5_EN (PIN6)	C_CK505_33M_PCI4	1	SRC5 DEFAULT
		0	CPU_STOP# and PCI_STOP#
PCIF5/ITP_EN (PIN7)	C_CK505_33M_PCI5	1	CPU_ITP
		0	SRC8 DEFAULT
PCI3/CFGF (PIN5)	C_CK505_33M_PCI3	LOW	See CFG Table DEFAULT (Set SATA and SRC come from PLL4)
		Mid	See CFG Table
		High	See CFG Table

SIO SMSC5545

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT
DTR1# [TEST_EN] /GP051 (PIN104)	O_DTR1#_R	1	PE BOOT Loader Strap (DTR1#)= Load from SPI
		0	PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT

PCH

On-Die PLL Voltage Regulator Voltage Select

HDA_SYNC	Description	
High	1.5V	DEFAULT
Low	1.8V	

On-Die PLL Voltage Regulator

GPIO28 (IN-PU)	Description	
High	Regulator is enabled.	DEFAULT
Low	Regulator is disabled.	

Topblock Swap Mode

GNT3#/GPIO55 (IN-PU)	Description	
High	Topblock swap mode: Disable	DEFAULT
Low	Topblock swap mode: Enable	

No Reboot Mode

SPKR (IN-PD)	Description	
High	No reboot mode: Enable	DEFAULT
Low	No reboot mode: Disable	

Integrated 1.05V VRM

INTVRMEN	Description	
High	Integrated 1.05V VRM: Enable	DEFAULT
Low	Integrated 1.05V VRM: Disable	

TLS Confidentiality

GPIO15 (IN-PD)	Description	
High	ME Crypto TLS cipher suite with confidentiality	DEFAULT
Low	ME Crypto TLS cipher suite with no confidentiality	

Flash Descriptor Override Strap

HDA_SDO	Description	
High	Flash descriptor security will be override	DEFAULT
Low	Disable ME in Manufacturing Mode	

DMI Rx Termination Voltage

SPI_MOSI (IN-PD)	Description	
Low	DMI Rx Termination Voltage	DEFAULT

DMI Termination Voltage

NV_CLE (IN-PU)	Description	
High	DMI and FDI Tx/Rx Termination Voltage	DEFAULT

Boot BIOS Destination Selection

GNT1# (IN-PU)	SATA1GP/GP19 (IN-PU)	Description	
Low	Low	Flash cycle routed to LPC	DEFAULT
High	Low	Flash cycle routed to PCI	
Low	High	Flash cycle routed to NAND	
High	High	Flash cycle routed to SPI	

Deep S4/S5 Well on-die Voltage Regulator Enable

DSWVRMEN	Description	
High	Enable	DEFAULT
Low	Disable	

Digital Port C Strap

DDPC_CTRLDATA	Description	
High	Configure Port C	DEFAULT
Low	Disable	

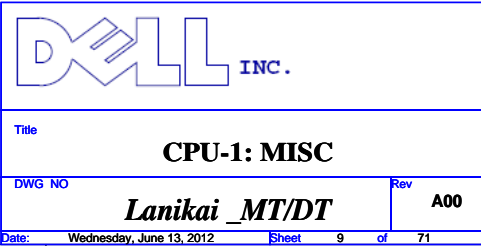
Title GPIO/IRQ/IDSEL Table	
DWG NO Lanikai_MT/DT	Rev A00
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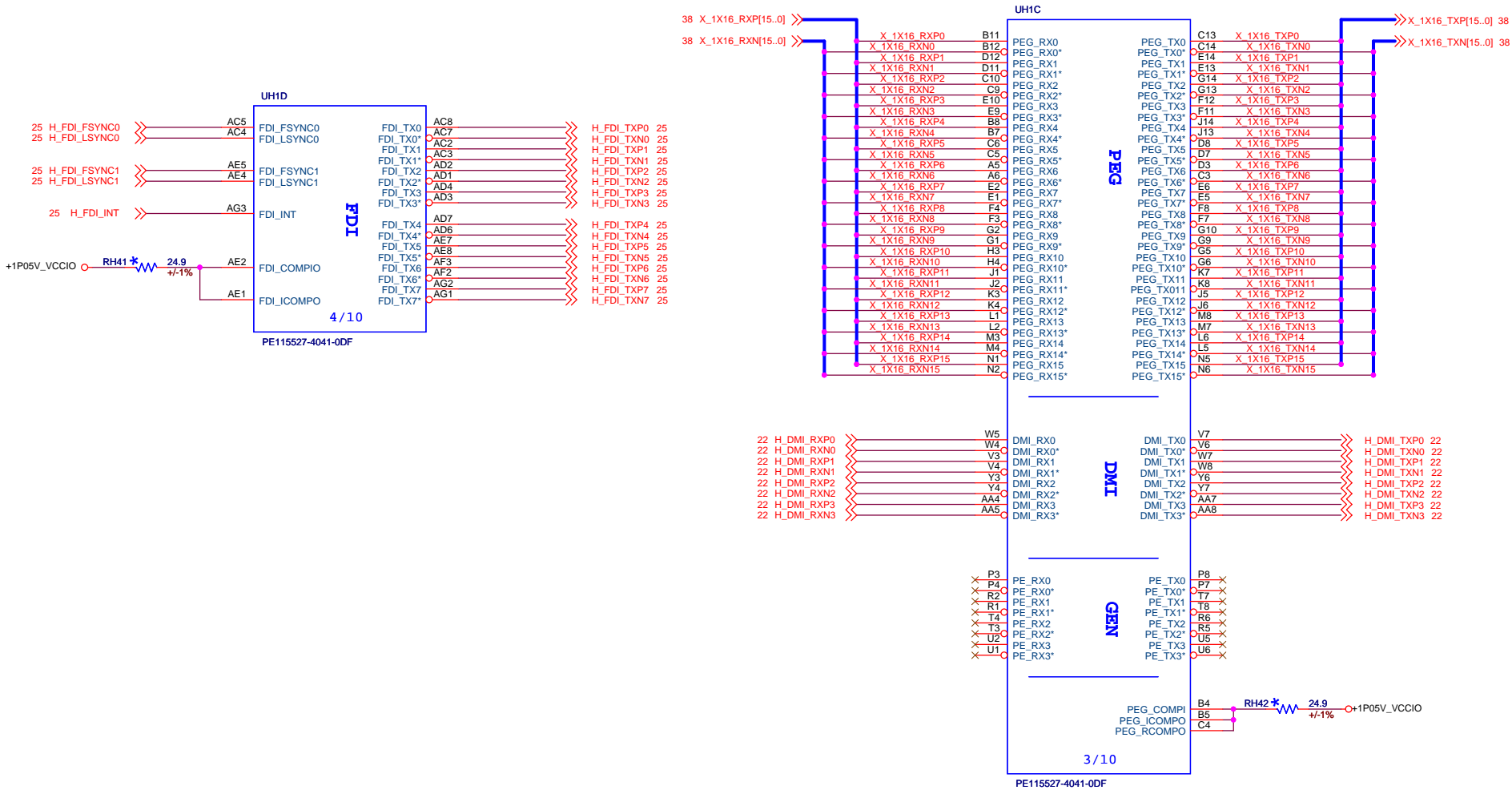
PCH GPIO Summary						
GPIO	Type	Power Well	Default	IN-PU/PD	EX-PU/PD	Schematic Usage
GPIO[0]	I/O	Core	GPI	--	10k pull-up to +3V	S_PECI_REG#
GPIO[1]	I/O	Core	GPI	20K IN-PU (only on TACH1)	10k pull-up to +3V (dummy) 1k pull-down to GND	S_OPL_CHASSIS_ID0
GPIO[2]	I/O	Core	GPI	--	8.2k pull-up to +3V	PCIE_MINI_CPUSE_DETECT#
GPIO[3]	I/O	Core	GPI	--	--	V_DDSF_C_HPD
GPIO[4]	I/O	Core	GPI	--	8.2k pull-up to +3V	V_GPL_VGA_CBL_DET#
GPIO[5]	I/O	Core	GPI	--	8.2k pull-up to +3V	PCIE_MINI_CPPE_DETECT#
GPIO[6]	I/O	Core	GPI	20K IN-PU (only on TACH2)	10k pull-up to +3V	S_OPL_PCH_HS_DET#
GPIO[7]	I/O	Core	GPI	20K IN-PU (only on TACH3)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_OPL_SKU2
GPIO[8]	I/O	Suspend	GPO	20K IN-PU	--	S_TP_0P8
GPIO[9]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5 (dummy)	U_USB_OC_R_#5
GPIO[10]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	X_WLAN_WAKE#
GPIO[11]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	X4_WAKE#
GPIO[12]	I/O	Suspend	Native	--	10k pull-up to +3V_LAN 10k pull-down to GND (dummy)	L_LAN_DISABLE#
GPIO[13]	I/O	Suspend	GPI	--	10k pull-up to +3V_S5	X1_WAKE#
GPIO[14]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5	GPO_WLOM
GPIO[15]	I/O	Suspend	GPO	20K IN-PD	1k pull-up to +3V_S5 (dummy)	S_PCH_OP15
GPIO[16]	I/O	Core	GPI	--	10k pull-up to +3V 10k pull-down to GND (dummy)	H_SKT0CC_R_#
GPIO[17]	I/O	Core	GPI	20K IN-PU (only on TACH0)	10k pull-up to +3V (dummy) 1k pull-down to GND	S_OPL_CHASSIS_ID1
GPIO[18]	I/O	Core	GPI	20K IN-PU	1k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	S_SATA10P
GPIO[19]	I/O	Core	Native	--	10k pull-up to +3V 10k pull-down to GND (dummy)	S_FLEXBAY_HDR_CBL_DET#
GPIO[20]	I/O	Core	GPI	--	10k pull-up to +3V (dummy) 10k pull-down to GND	S_OPL_BRD_REV0
GPIO[21]	I/O	Core	GPI	--	1k pull-up to +3V 4.7k pull-down to GND (dummy)	S_PCH_CONFIG_JUMPER
GPIO[22]	I/O	Core	Native	20K IN-PU	10k pull-up to +3V (dummy)	L_DRG1#
GPIO[24]	I/O	Suspend	GPO	--	100k pull-up to +3V_S5	H_SKT0CC#
GPIO[27]	I/O	Deep Sleep	GPI	20K IN-PU	10k pull-up to +3V_DUAL 1k pull-down to GND (dummy)	S_OP27_PD
GPIO[28]	I/O	Suspend	GPO	20K IN-PU	10k pull-up to +3V_S5 1k pull-down to GND (dummy)	S_PCH_GP28_PU
GPIO[29]	I/O	Suspend	Native	--	1k pull-up to +3V_S5 (dummy)	S_SLP_LAN#
GPIO[30]	I/O	Deep Sleep	Native	--	10k pull-up to +3V_DUAL (dummy) 1k pull-down to GND (dummy)	S_SUSWARN#
GPIO[31]	I/O	Deep Sleep	GPI	TBD IN-PD	8.2k pull-up to +3V_DUAL	S_PSYD_CLR
GPIO[32]	I/O	Core	GPO	--	10k pull-up to +3V (dummy) 220 pull-down to GND	S_OPL_SKU0
GPIO[33]	I/O	Core	GPO	--	--	--
GPIO[34]	I/O	Core	GPI	--	10k pull-up to +3V	PCH_GPIO34
GPIO[35]	I/O	Core	GPO	--	10k pull-up to +3V (dummy) 220 pull-down to GND	S_OPL_SKU1
GPIO[36]	I/O	Core	GPI	20K IN-PD	--	S_PCH_OP36
GPIO[37]	I/O	Core	GPI	20K IN-PD	--	S_PCH_OP37
GPIO[38]	I/O	Core	GPI	--	10k pull-up to +3V (dummy) 10k pull-down to GND	S_OPL_CHASSIS_ID2
GPIO[39]	I/O	Core	GPI	--	10k pull-up to +3V	A_FP_PRES#
GPIO[40]	I/O	Suspend	Native	--	--	U_USB_OC_R_#1

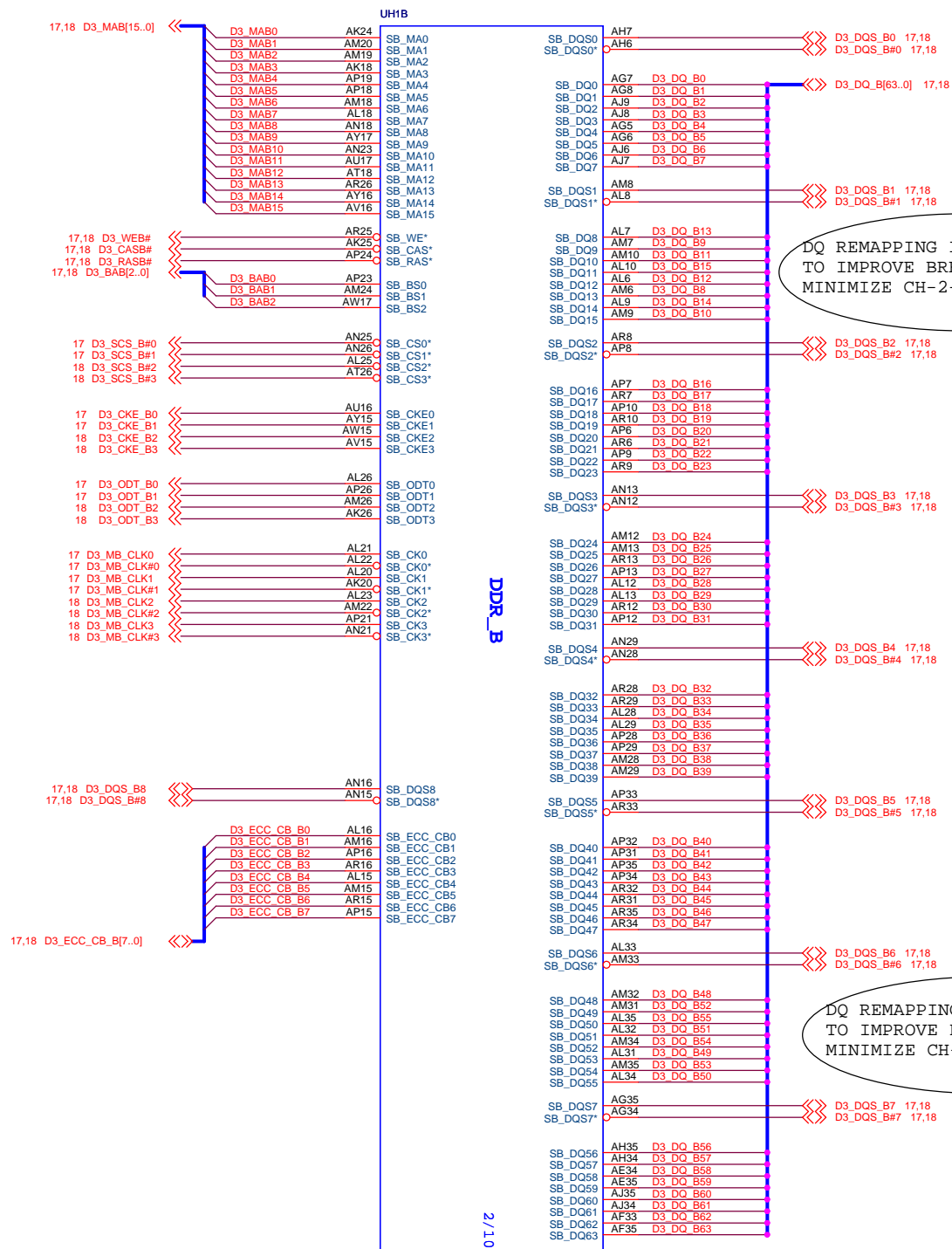
GPIO[41]	I/O	Suspend	Native	--	--	U_USB_OC_R_#2
GPIO[42]	I/O	Suspend	Native	--	--	U_USB_OC_R_#3
GPIO[43]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5 (dummy)	U_USB_OC_R_#4
GPIO[44]	I/O	Suspend	Native	20K IN-PU	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	S_INTRUD_CBL_DET#
GPIO[45]	I/O	Suspend	Native	--	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	O_COM_SER2_DET#
GPIO[46]	I/O	Suspend	Native	20K IN-PU	10k pull-up to +3V_S5 (dummy) 1k pull-down to GND	S_OPL_BRD_REV1
GPIO[48]	I/O	Core	GPI	--	10k pull-up to +3V	S_OPIO48_PU
GPIO[49]	I/O	Core	GPI	--	8.2k pull-up to +3V	TMIN_SHIFT
GPIO[50]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#1
GPIO[51]	I/O	Core	Native	20K IN-PU	1k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	K_GNT#1
GPIO[52]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#2
GPIO[53]	I/O	Core	Native	20K IN-PU	1k pull-down to GND (dummy)	K_GNT#2
GPIO[54]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#3
GPIO[55]	I/O	Core	Native	20K IN-PU	1k pull-down to GND (dummy)	K_GNT#3
GPIO[57]	I/O	Suspend	GPI	--	10k pull-up to +3V_S5 (dummy) 47k pull-down to GND	S_OPIO57_PD
GPIO[58]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_SMLINK1_CLK
GPIO[59]	I/O	Suspend	Native	--	--	U_USB_OC_R_#0
GPIO[60]	I/O	Suspend	Native	--	2.2k pull-up to +3V_S5	GPIO_WIRELESS_DISABLE#
GPIO[61]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5 (dummy)	S_LPCPD#
GPIO[62]	I/O	Suspend	Native	--	--	S_SUSCLK
GPIO[63]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_PCIAUX_GATE
GPIO[64]	I/O	Core	Native	20K IN-PD	--	S_TP_CLKOUTFLEX0
GPIO[65]	I/O	Core	Native	20K IN-PD	--	C_14M_SIO_R
GPIO[66]	I/O	Core	Native	20K IN-PD	--	S_TP_CLKOUTFLEX2
GPIO[67]	I/O	Core	Native	20K IN-PD	--	C_14M_TPM_R
GPIO[68]	I/O	Core	GPI	20K IN-PU (only on TACH4)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_OPL_BRD_REV2
GPIO[69]	I/O	Core	GPI	20K IN-PU (only on TACH5)	10k pull-up to +3V	O_PRT_DET#
GPIO[70]	I/O	Core	Native	20K IN-PU (only on TACH6)	8.2k pull-up to +3V	S_FP_CHAS_DET#
GPIO[71]	I/O	Core	Native	20K IN-PU (only on TACH7)	10k pull-up to +3V	--
GPIO[72]	I/O	Suspend	Native (Mobile Only)	20K IN-PU	10k pull-up to +3V_S5	S_PCH_OP72_PU
GPIO[74]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_MFG_MODE_OR
GPIO[75]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_SMLINK1_DATA

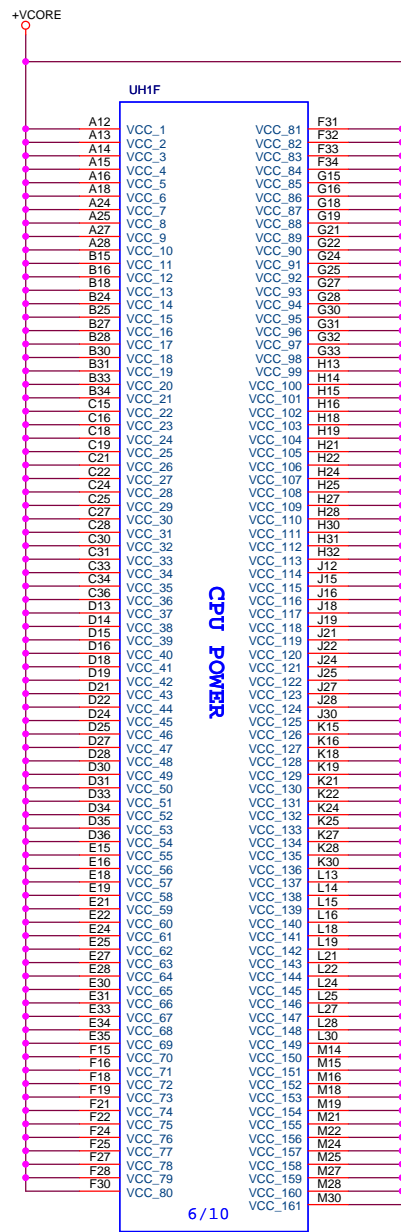
GPIO	PIN NAME	Power well	Buffer Type	EX-PU/PD	Signal Name
OP000	(DIA0_LED3#) OP000	VTR	I/O	NA	O_DIA0_LED3#
OP001	(DIA0_LED1#) OP001	VTR	I/O	NA	O_DIA0_LED1#
OP002	(DIA0_LED2#) OP002	VTR	I/O	NA	O_DIA0_LED2#
OP003	(DIA0_LED4#) OP003	VTR	I/O	NA	O_DIA0_LED4#
OP004	OP004	VTR	I/O	NA	NC
OP005	(H_CUPRST#) OP005 / PECIAL_REQUEST#	VTR	I/O/D	10k pull-up to +3V	O_PECIAL_REQ#
OP006	YELLOW# / OP006	VTR	O/O	NA	O_YELLOW#
OP007	GREEN# / OP007	VTR	O/O	NA	O_GREEN#
OP010	SMODAT2 / OP010	VTR	I/O/D	0.2k pull-up to +3V_DUAL (dummy)	S_SMLINK1_DATA_R
OP011	SMBCLK2 / OP011	VTR	I/O/D	8.2k pull-up to +3V_DUAL (dummy)	S_SMLINK1_CLK_R
OP012	OP012	VTR	I/O	8.2k pull-up to +3V_DUAL	SPL_DI
OP013	OP013	VTR	I/O	NA	NC
OP014	(TMIN_SHIFT) OP014	VTR	I/O	8.2k pull-up to +3V	TMIN_SHIFT
OP015	PWRBTN# / OP015	VTR	I/O	1k pull-up to +3V_DUAL	O_PWRBTN#
OP016	PROCHOT_IN# / PROCHOT_OUT# / OP016	VTR	I/O/D/O	51 ohm pull-up to +1P05V_VCCIO	H_PROCHOT#
OP017	TACH1 / OP017	VTR	I/O	1k pull-up to +3V	O_SEN_CPUFAN
OP020	TACH2 / OP020	VTR	I/O	1k pull-up to +3V	O_SEN_CHAFAN
OP021	TACH3 / OP021	VTR	I/O	NA	NC
OP022	PWM1 / OP022	VTR	O/O	4.7k pull-up to +3V	O_CPUFAN_PWM
OP023	PWM2 / OP023	VTR	O/O	4.7k pull-up to +3V	O_CHAFAN_PWM
OP024	PWM3 / OP024	VTR	O/O	NA	NC
OP025	(FP_CBL_DET#) OP025	VTR	I/O	8.2k pull-up to +3V_S5	O_FP_CBL_DET#
OP026	PCL_RST_S5# / OP026	VTR	O/O	NA	X_PCL_RST_PCH_SLOT#
OP027	PCL_RST_SLOTS# / OP027	VTR	O/O	NA	H_RESET#
OP030	PS_ON# / OP030	VTR	O/O	4.7k pull-up to +5VSB	O_PSON#
OP031	(PC_SPHR_DET) OP031	VTR	I/O	8.2k pull-up to +3V_DUAL	O_AUD_PCSPHR_DET#
OP032	OP032	VTR	I/O	NA	NC
OP033	PWR_GOOD_3V / OP033	VTR	O/O	NA	PWRGD_3V
OP034	RSNRST# / OP034	VTR	O/O	10k pull-down to GND	O_RSNRST#
OP035	OP035	VTR	I/O	8.2k pull-up to +3V_DUAL	O_BC_CLK
OP036	(OP036 / SMB_CLK1)	VTR	I/O/D	8.2k pull-up to +3V_DUAL (dummy)	S_SMBCLK_PCL_R
OP040	OP040 / SMB_DAT1	VTR	I/O/D	8.2k pull-up to +3V_DUAL (dummy)	S_SMBDATA_PCL_R
OP041	OP041 / IO_FME#	VTR	I/O/D	10k pull-up to +3V_S5	O_IO_FME#
OP042	OP042 / DRV0EN0	VTR	I/O	100k pull-up to +3V_DUAL (dummy)	T_ESATA_DET#
OP043	DCD1# / OP043 / MCDAT	VTR	I/O/O	NA	O_DCD1#_R
OP044	DSR1# / OP044 / MCLK	VTR	I/O/O	NA	O_DSR1#_R
OP045	RxD1 / OP045	VTR	I/O	NA	O_RxD1_R
OP046	RTS1# / OP046	VTR	O/O	NA	O_RTS1#_R
OP047	(SV_PSRNT) OP047 / TXD1	VTR	I/O	NA	O_TXD1_R
OP050	CTS1# / OP050	VTR	I/O	NA	O_CTS1#_R
OP051	DTR1# / TEST_EN# / OP051	VTR	O/O	8.2k pull-up to +3V_DUAL (dummy) 30k pull-down to GND	O_DTR1#_R
OP052	R1# / OP052	VTR	I/O	NA	O_R1#_R
OP053	OP053 / DCD2#	VTR	I/O	2.2k pull-up to +3V	O_DCD2#_R
OP054	OP054 / DSR2#	VTR	I/O	2.2k pull-up to +3V	O_DSR2#_R
OP055	OP055 / RxD2	VTR	I/O	2.2k pull-up to +3V	O_RxD2_R
OP056	(PWR2_PSRNT) OP056 / RTS2#	VTR	I/O	30k pull-up to +3V	O_RTS2#_R
OP057	(MB_RE0_P0) OP057 / TXD2	VTR	I/O	30k pull-up to +3V	O_TXD2_R
OP058	OP058 / CTS2#	VTR	I/O	2.2k pull-up to +3V	O_CTS2#_R
OP061	(MEM_RE0_P0) OP061 / DTR2#	VTR	I/O	30k pull-up to +3V	O_DTR2#_R
OP062	OP062 / R12#	VTR	I/O	2.2k pull-up to +3V	O_R12#_R
OP063	OP063 / XBORST#	VTR	I/O/D	10k pull-up to +3V	O_XBORST#
OP064	OP064 / A20M	VTR	I/O/D	10k pull-up to +3V	O_A20
OP065	SLP_S3# / OP065	VTR	I/O	NA	S_SLP_S3#
OP066	SLP_S4_S5# / OP066	VTR	I/O	NA	S_SLP_S4#
OP067	PWRD_P5 / OP067	VTR	I/O	1k pull-up to +5V	B_ATT_PWROK
OP070	SPEAKER [DIA0_EN#] / OP070	VTR	O/O	8.2k pull-up to +3V_DUAL (dummy) 8.2k pull-down to GND	O_SPEAKER
OP071	(SLP_M#) OP071 / IO_SMI#	VTR	I/O/D	NA	S_SLP_M#
OP072	PECL1 / LVSBM_CLK1 / OP072	VTR	PECL1/O/I/O	1k pull-up to +1P05V_VCCIO (dummy)	H_PEC1_R
OP073	PECL_READY / LVSBM_DAT1 / OP073	VTR	PECL1/O/I/O	1k pull-up to +1P05V_VCCIO	O_OP73_PU





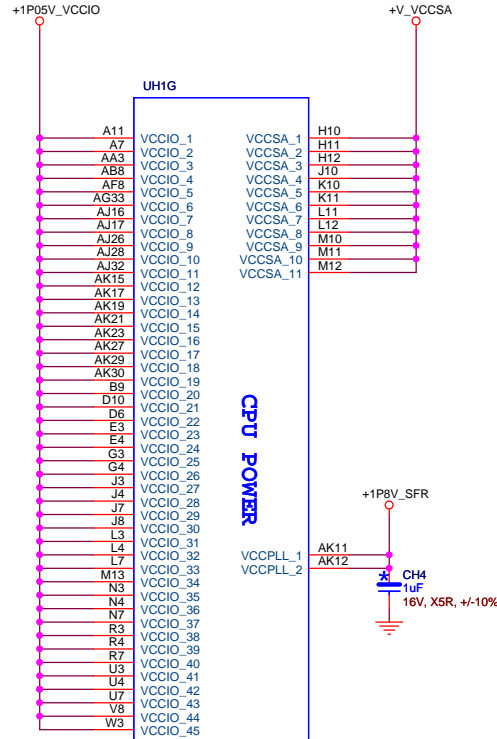






PE115527-4041-0DF

6/10

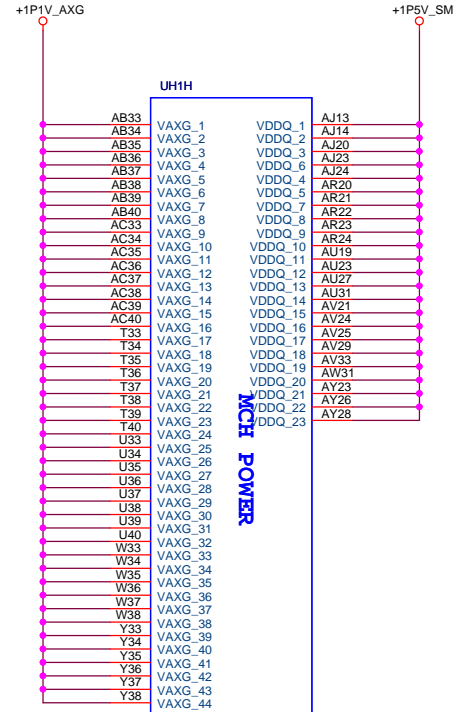
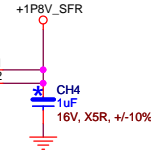


CPU POWER

VCCPLL_1
VCCPLL_2

7/10

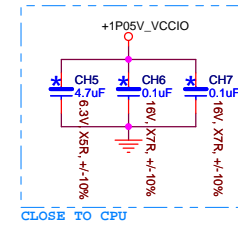
PE115527-4041-0DF



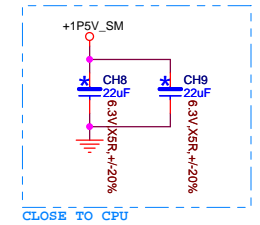
MCH POWER

8/10

PE115527-4041-0DF



CLOSE TO CPU



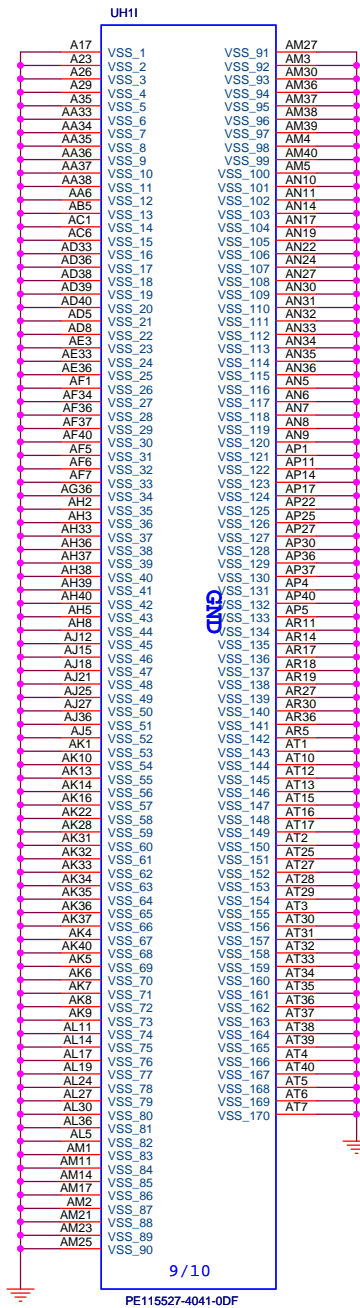
CLOSE TO CPU

DELL INC.

Title: **CPU-5: Power**

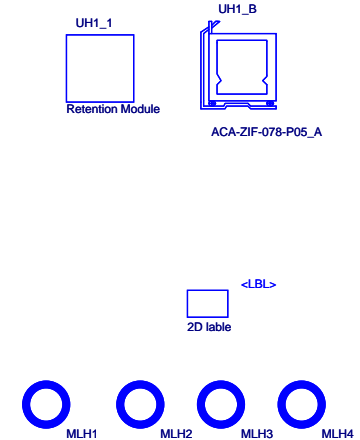
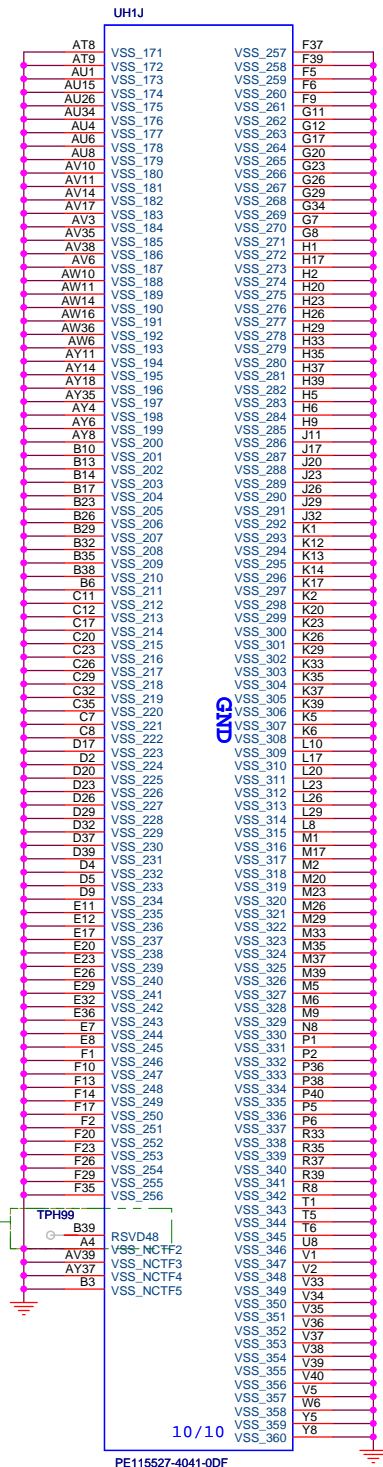
DWG NO: **Lanikai_MT/DT** Rev: **A00**

Date: Wednesday, June 13, 2012 Sheet: 13 of 71



B39 update to RSVD48;
PDG 0.7-12/07/09

EDS: B39 defined "VSS_NCTF"
CRB: B39 defined "RSVD"
pin_B39 follow CRB pin define;
CRB 0.7-12/10/09



DELL INC.

Title

CPU-6: GND

DWG NO

Lanikai MT/DT

Rev

A00

Date: Wednesday, June 13, 2012

Sheet 14 of 71

SMB ADDRESS:000



D3_WEA#	11,16
D3_RASA#	11,16
D3_CASA#	11,16
D3_RESET#	11,16,17,18

```

16,17,18,32,52 S_SMBCLK_MAIN
16,17,18,32,52 S_SMBDATA_MAIN
SA_BS[0]-->Pin 71 (BA0)
SA_BS[1]-->Pin 190 (BA1)
SA_BS[2]-->Pin 52 (BA2)
; CRB 0.7-12/10/09

```

20100104: Remove CD5 10uF

The image displays two circuit diagrams for a power supply rail, showing the removal of capacitors CD11 and CD12, and the addition of capacitors CD13, CD14, and CD51.

Top Diagram (Initial State):

- Input: +1P5V_SM
- Resistor RD1: 1K, tolerance +/-1%
- Capacitor CD11: 0.1uF, 16V, X7R, tolerance +/-10% (to be removed)
- Resistor RD2: 1K, tolerance +/-1%
- Capacitor CD12: 0.1uF, 16V, X7R, tolerance +/-10% (to be removed)
- Output: D3_DQ_VREF_A 16

Bottom Diagram (Final State):

- Input: +1P5V_SM
- Resistor RD3: 1K, tolerance +/-1%
- Capacitor CD13: 0.1uF, 16V, X7R, tolerance +/-10% (to be added)
- Resistor RD4: 1K, tolerance +/-1%
- Capacitor CD14: 0.1uF, 16V, X7R, tolerance +/-10% (to be added)
- Capacitor CD51: 2.2uF, 6.3V, Y5V, tolerance +/-20% (to be added)
- Output: D3_CA_VREF_A 16

Change Log:

Change	Reason
Add CD52, CD53	follow CRB 0.7-12/28/09
Del CD52, CD53	12-29/09
Change to 0.1uF	PDG 0.7-12/07/09
Add CD47	CD CRB 0.7-12/10
Del CD47	CD CRB 0.7-12/29

```
Add CD47 , CD48, CD49, CD50, CD51 and Dummy;  
CRB 0.7-12/10/09  
  
Del CD47 , CD48, CD49, CD50, CD51 and Dummy;  
CRB 0.7-12/29/09
```

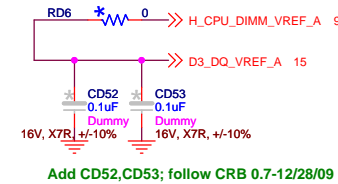
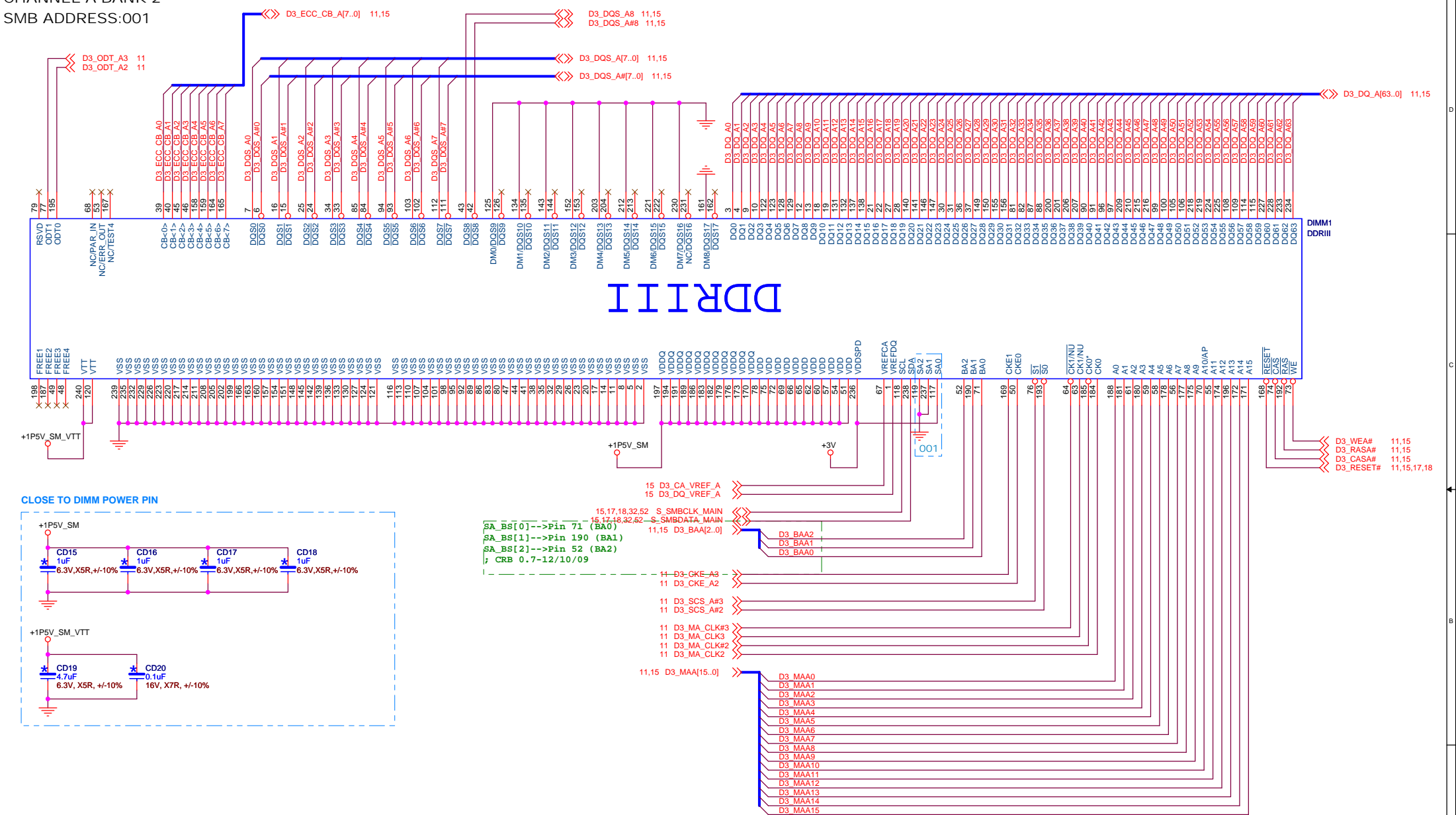


Title **DDR3 Conn: CHA_1 (DIMM3)**

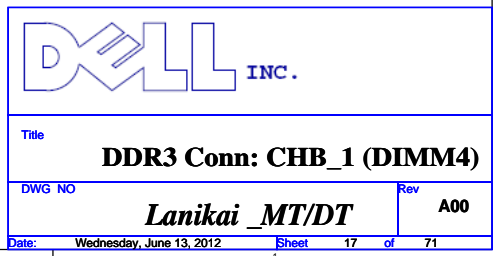
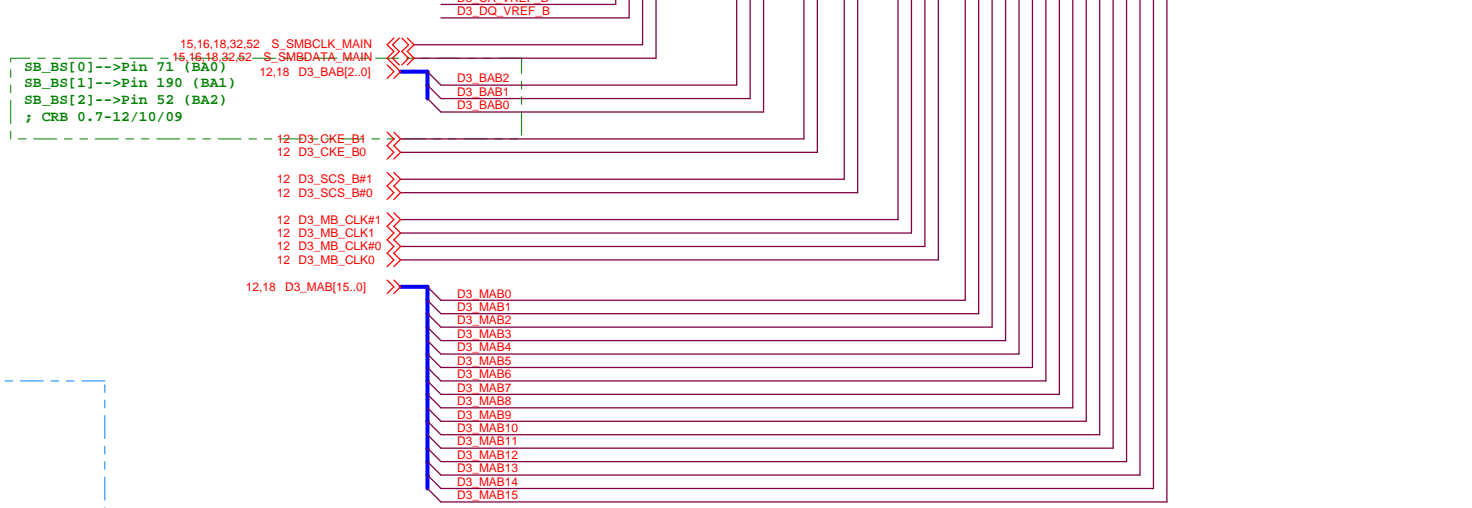
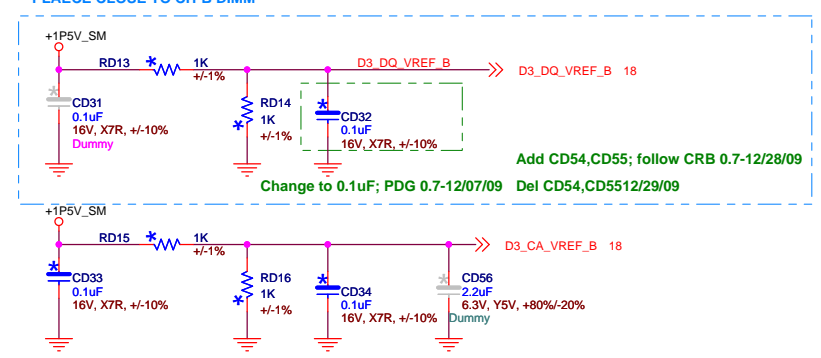
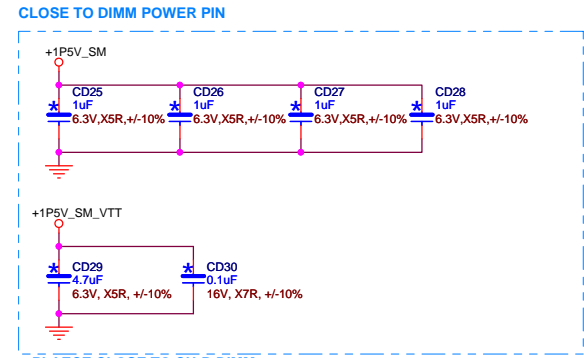
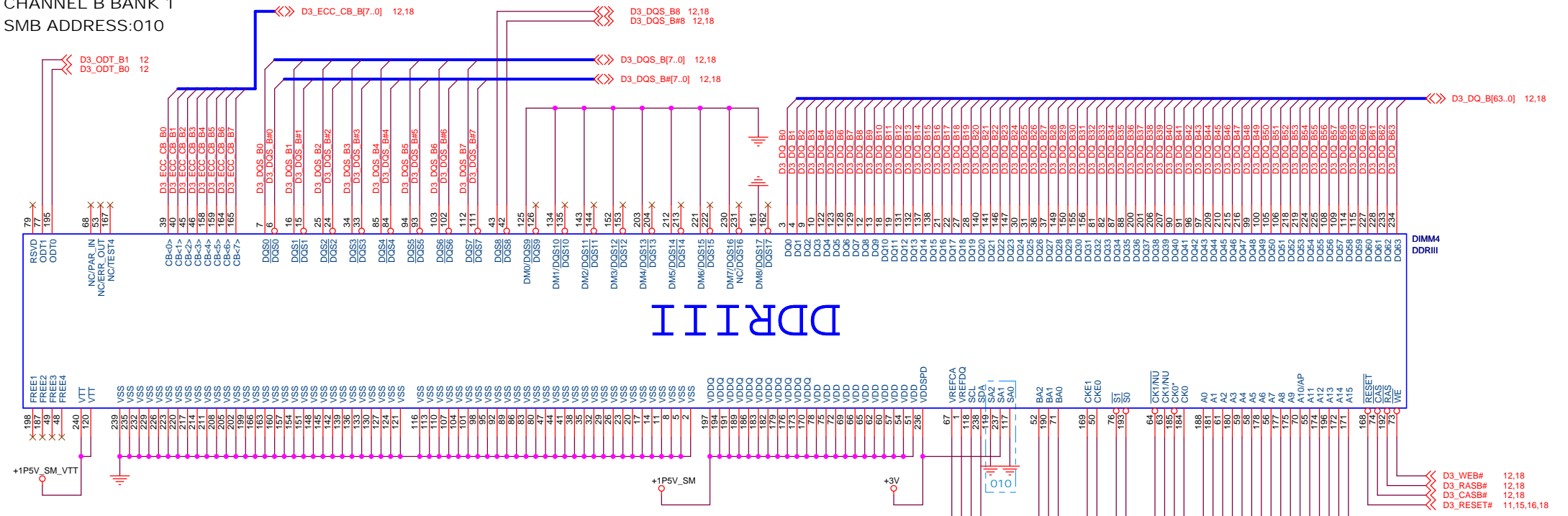
DWG NO	Rev
1001-1002 MT/DT	A00

Date: Wednesday, June 13, 2012 Sheet 15 of 71

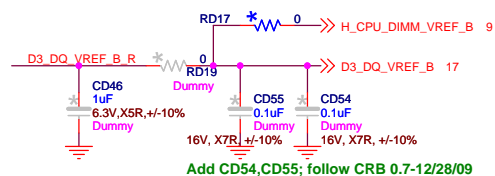
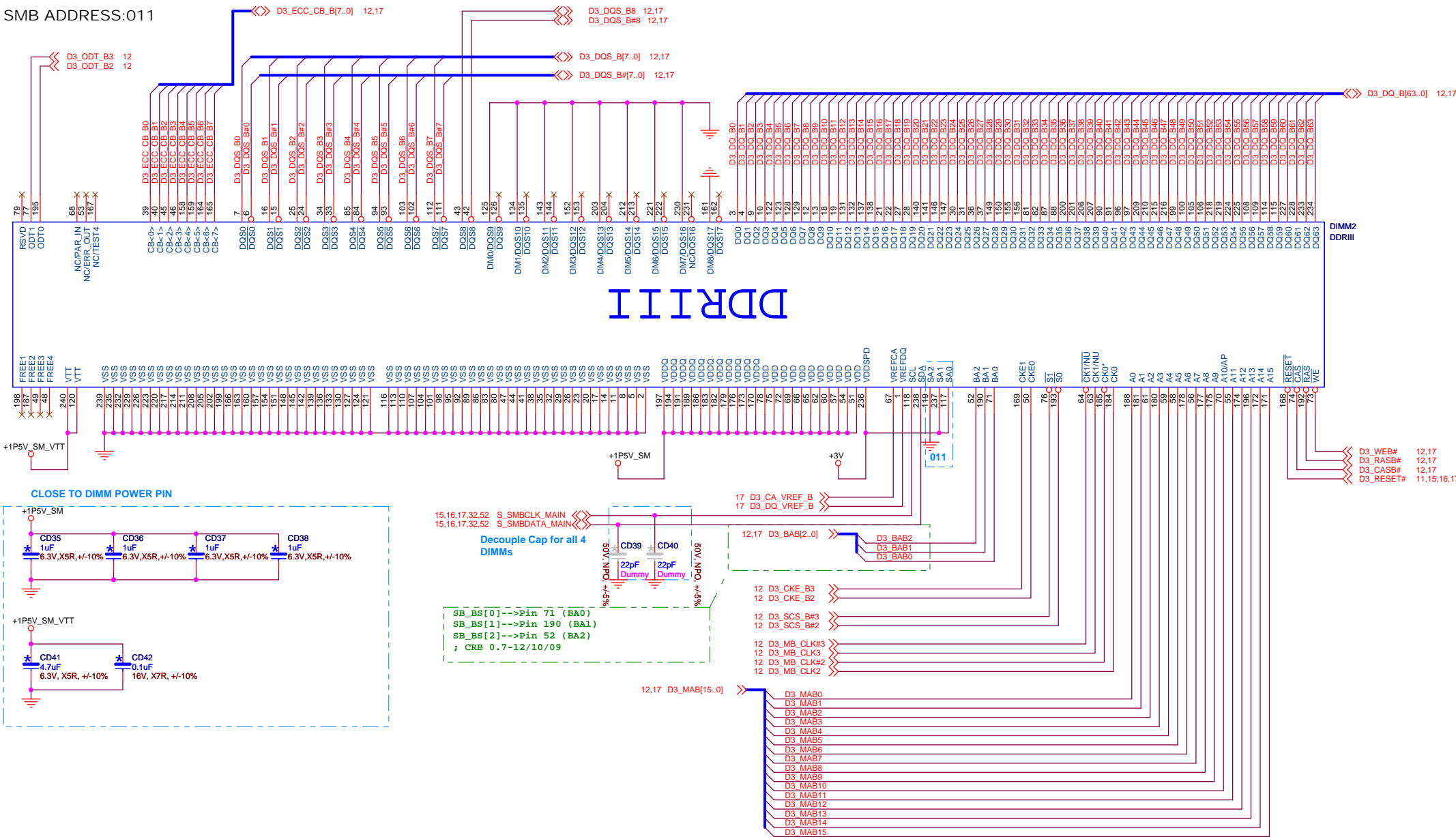
CHANNEL A BANK 2
SMB ADDRESS:001



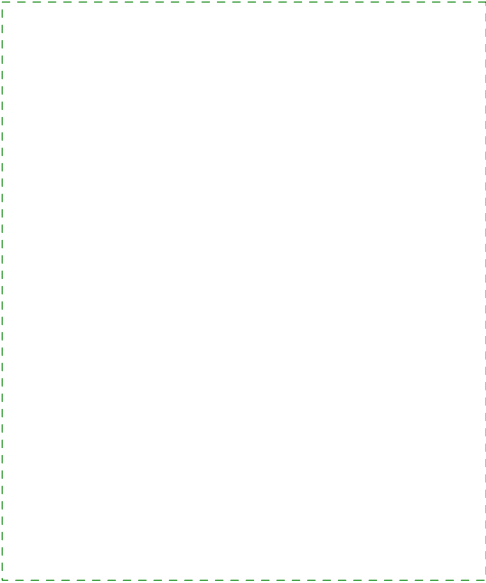
CHANNEL B BANK 1
SMB ADDRESS:010



CHANNEL B BANK 2
SMB ADDRESS:011



20100106: Remove ONFI function since not support



Title
TBD

DWG NO	<i>Lanikai_MT/DT</i>	Rev	A00
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Date:	Wednesday, June 13, 2012	Sheet	19	of	71
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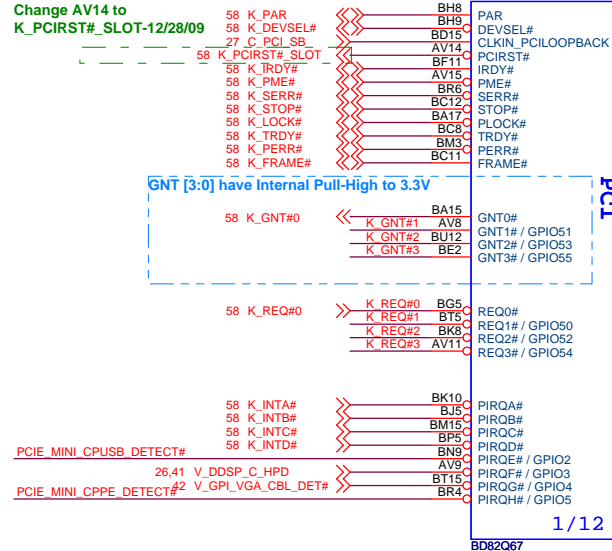


Title	
Clock GEN	

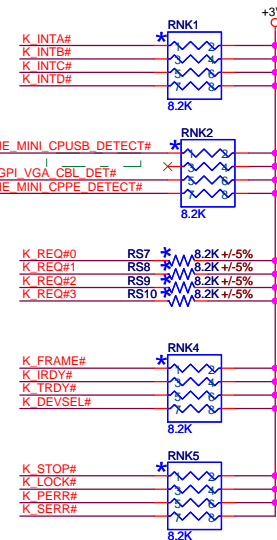
DWG NO	Rev
<i>Lanikai_MT/DT</i>	A00

Date:	Wednesday, June 13, 2012	Sheet	20	of	71
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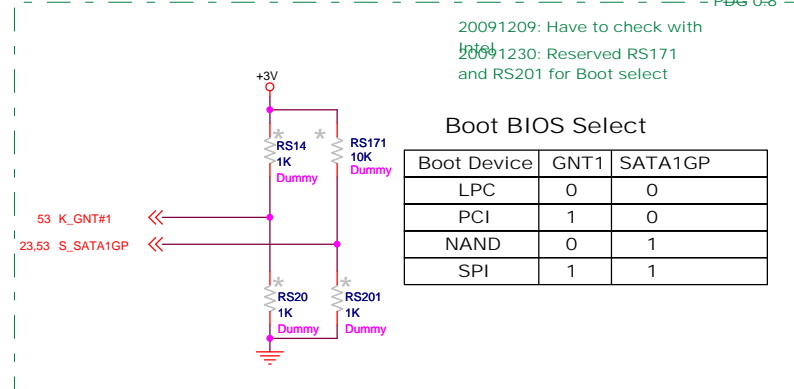
Change AV14 to
K_PCIRST#_SLOT-12/28/09



K_INTF# change to
V_DDSP_C_HPDP-12/30/09
20100108: Remove
V_DDSP_C_HPDP pull-up



Left biotth SATA/GPIO19 and GNT1# floating.
No pull up required for Default(SPI)



Boot BIOS Select

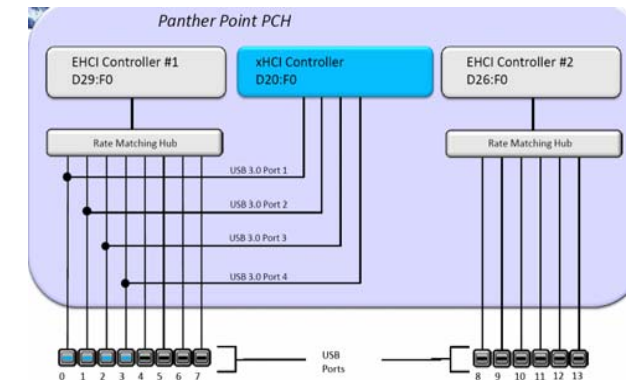
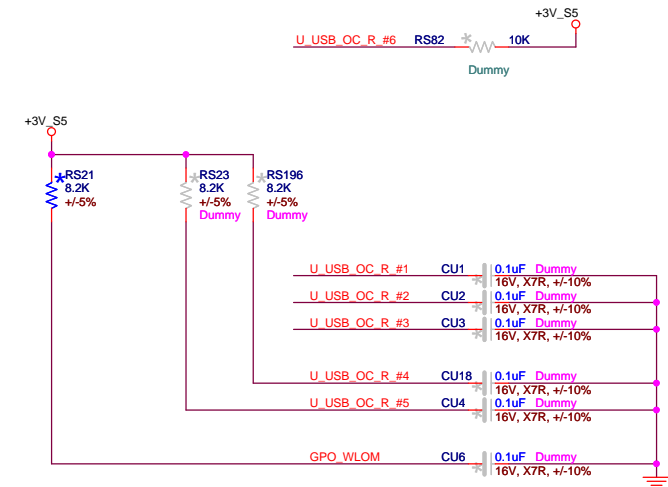
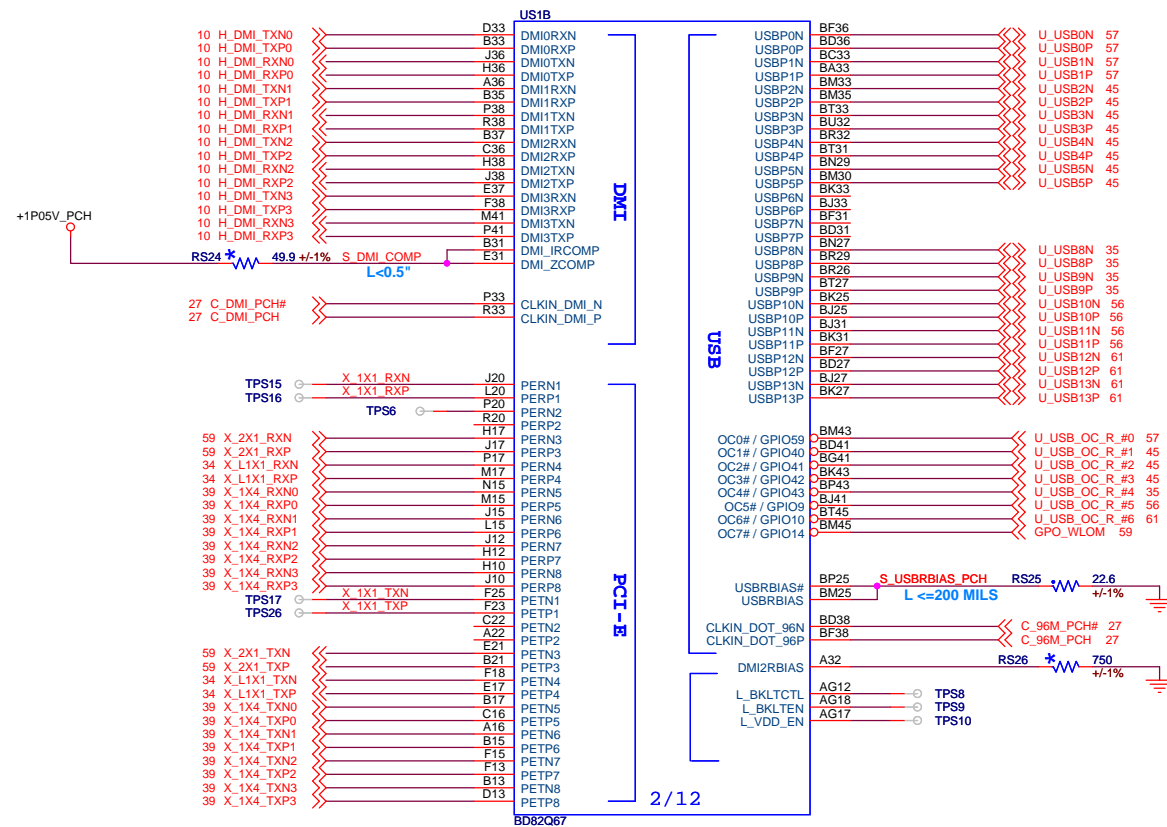
Boot Device	GNT1	SATA1GP
LPC	0	0
PCI	1	0
NAND	0	1
SPI	1	1

GNT3# Internal pull-up.



DG 0.7
GNT3 is top block swap mode:
connect to ground with 4.7k ohm weak
pull down resistor for top block swap mode
GNT2#/GPIO53:ESI strap for server platform
ONLY,Do not pull low.





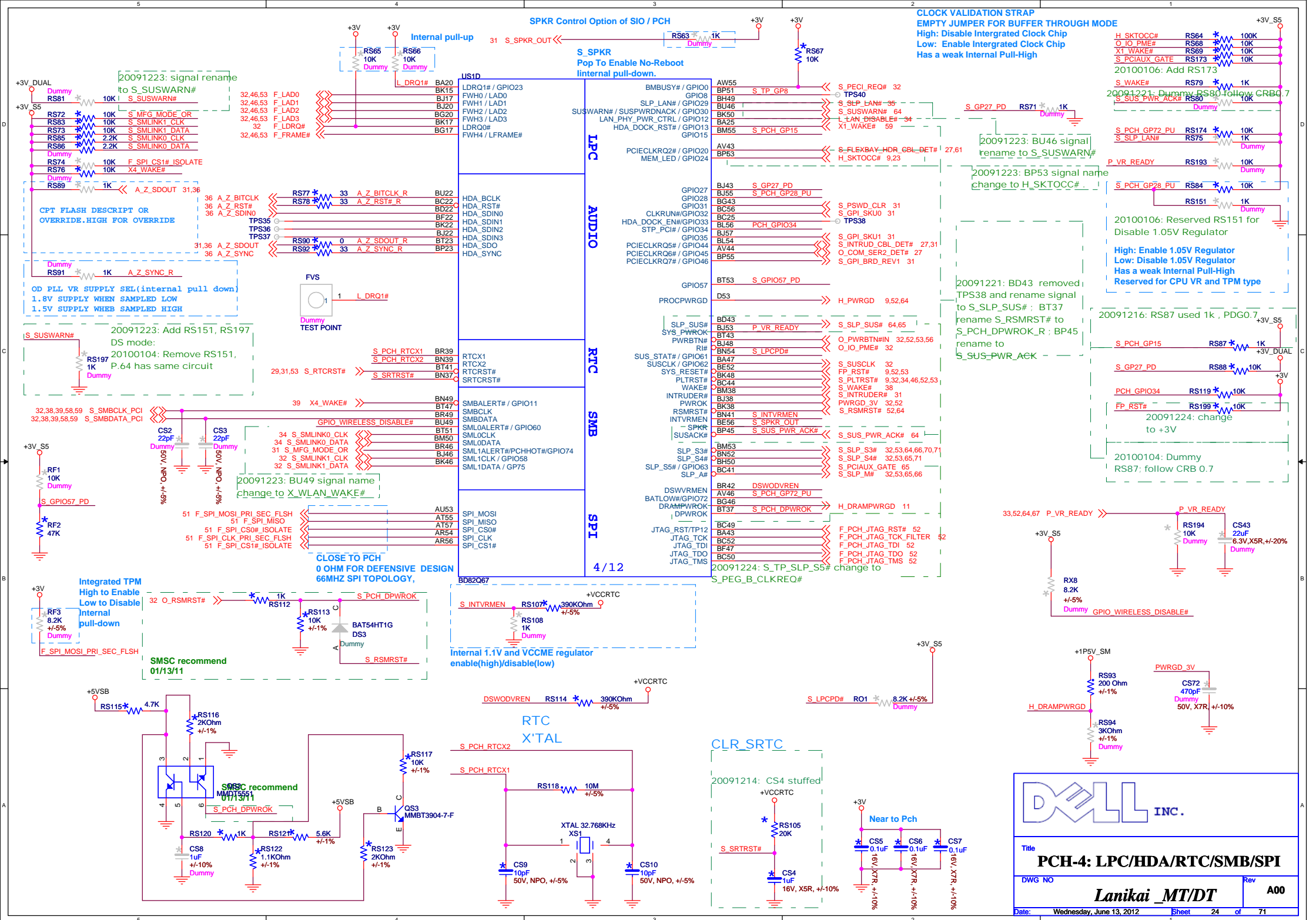
USB2.0	USB3.0	Lainikai OC Pin	Power	Function	Standard OC pin configuration
Port 0	U_USB0N U_USB0P	Port 1	USBPWR1_F_50	Front USB3.0	OC0#
Port 1	U_USB1N U_USB1P	Port 2	USBPWR2_F_50	Front USB3.0	OC0#
Port 2	U_USB2N U_USB2P	Port 3	USBPWR3_F_50	Rear USB3.0	OC1#
Port 3	U_USB3N U_USB3P	Port 4	USBPWR4_F_50	Rear USB3.0	OC1#
Port 4	U_USB4N U_USB4P				
Port 5	U_USB5N U_USB5P				
Port 6	U_USB6N U_USB6P				
Port 7	U_USB7N U_USB7P				
Port 8	U_USB8N U_USB8P				
Port 9	U_USB9N U_USB9P				
Port 10	U_USB10N U_USB10P				
Port 11	U_USB11N U_USB11P				
Port 12	U_USB12N U_USB12P				
Port 13	U_USB13N U_USB13P				

Intel

PCH-2: DMI/PCIe/USB

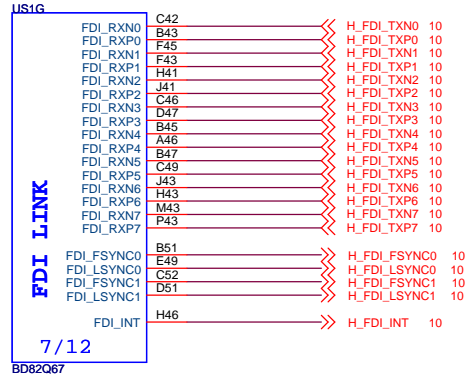
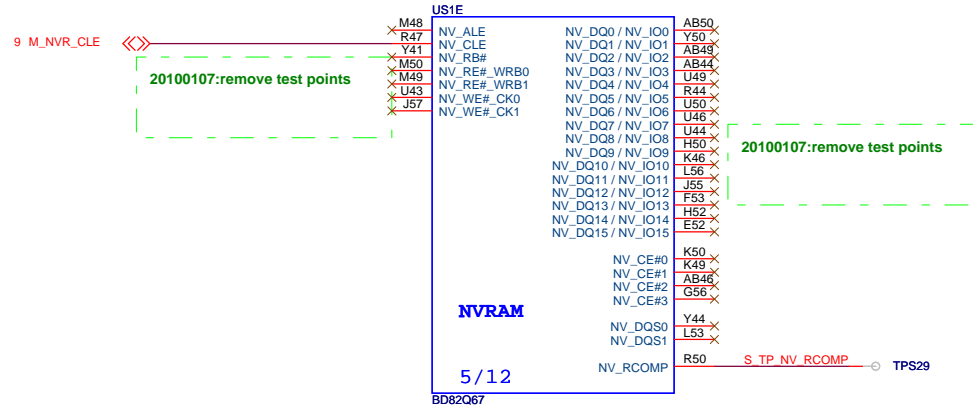
DWG NO **Lanikai MT/DT** Rev **A00**

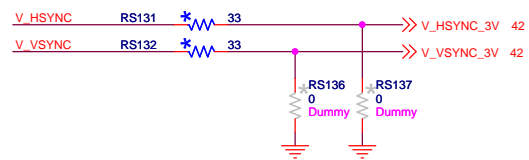
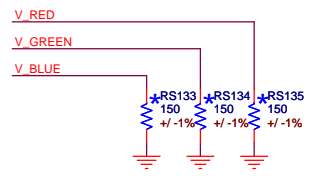
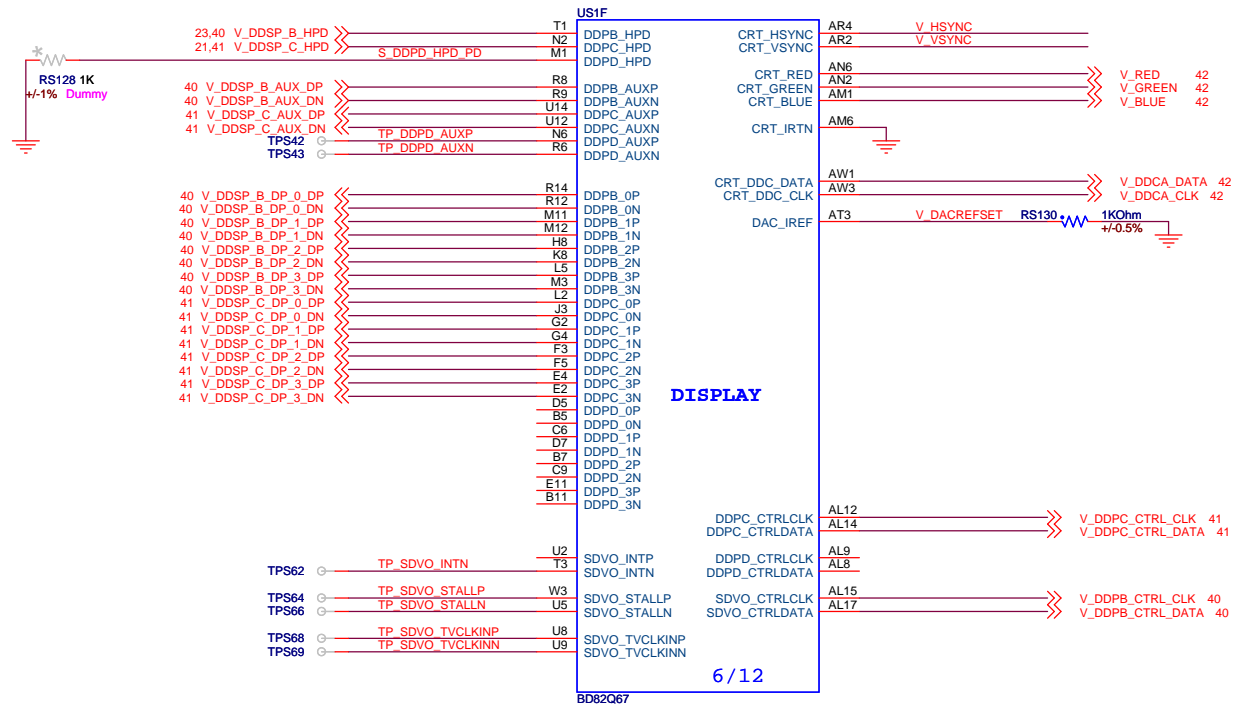
Date: Wednesday, June 13, 2012 Sheet 22 of 71



20100106: Remove ONFI function since not support

S_NVR_CLE internal pull-down.





Intel

Title

PCH-6: Display

DWG NO

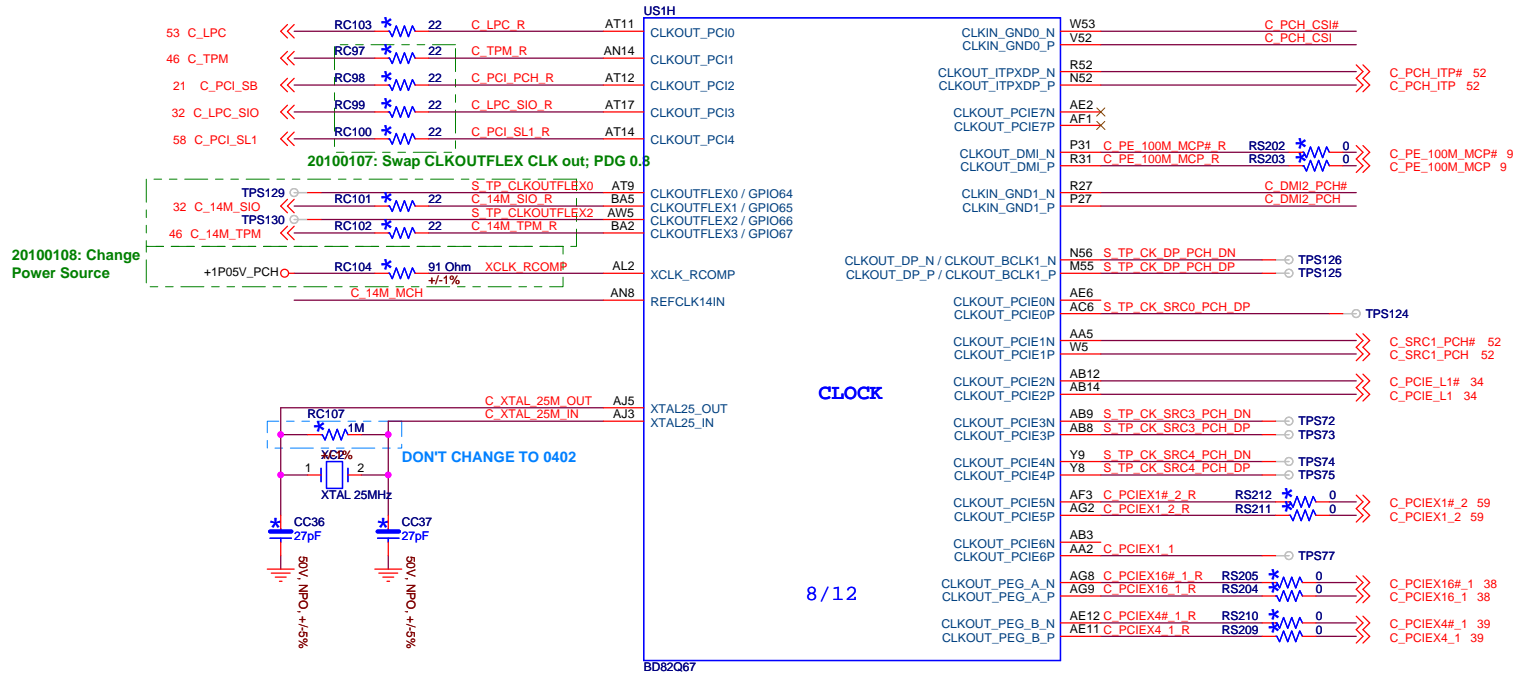
Rev

A00

Date: Wednesday, June 13, 2012

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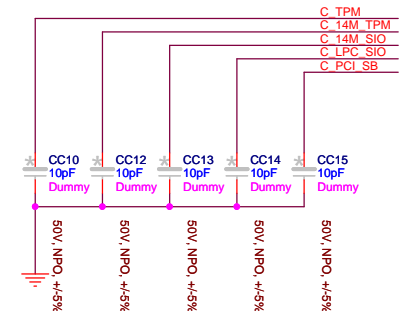
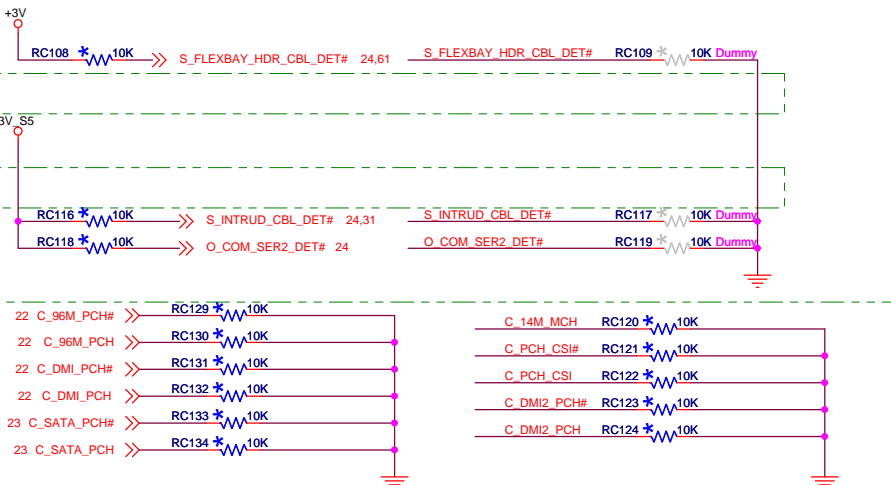
20100106: Remove RS96; CRB 0.7
 20100106: Swap C_PCH_PCIE0_R and C_PCH_PCIE1_R; CRB 0.7
 20100106: Disconnect AT11 and left Test point; CRB 0.7

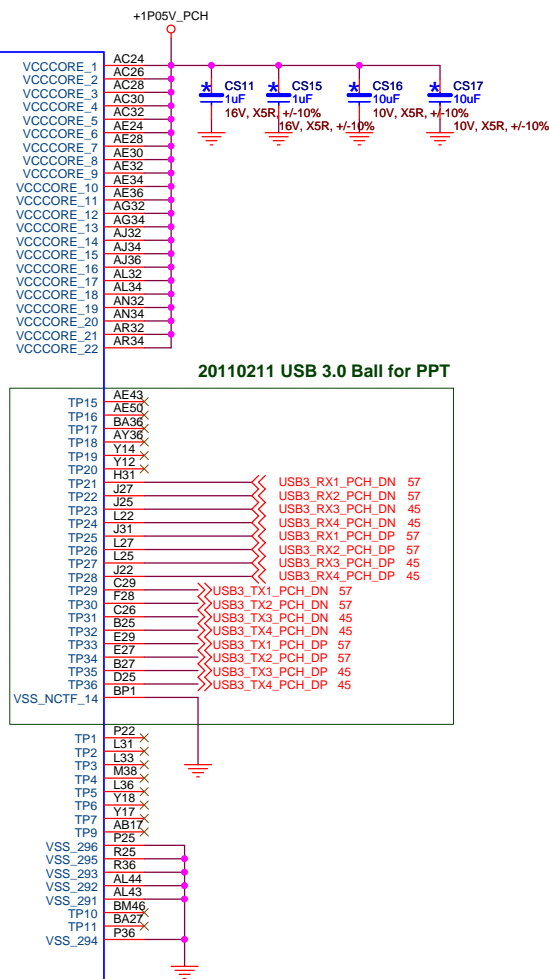
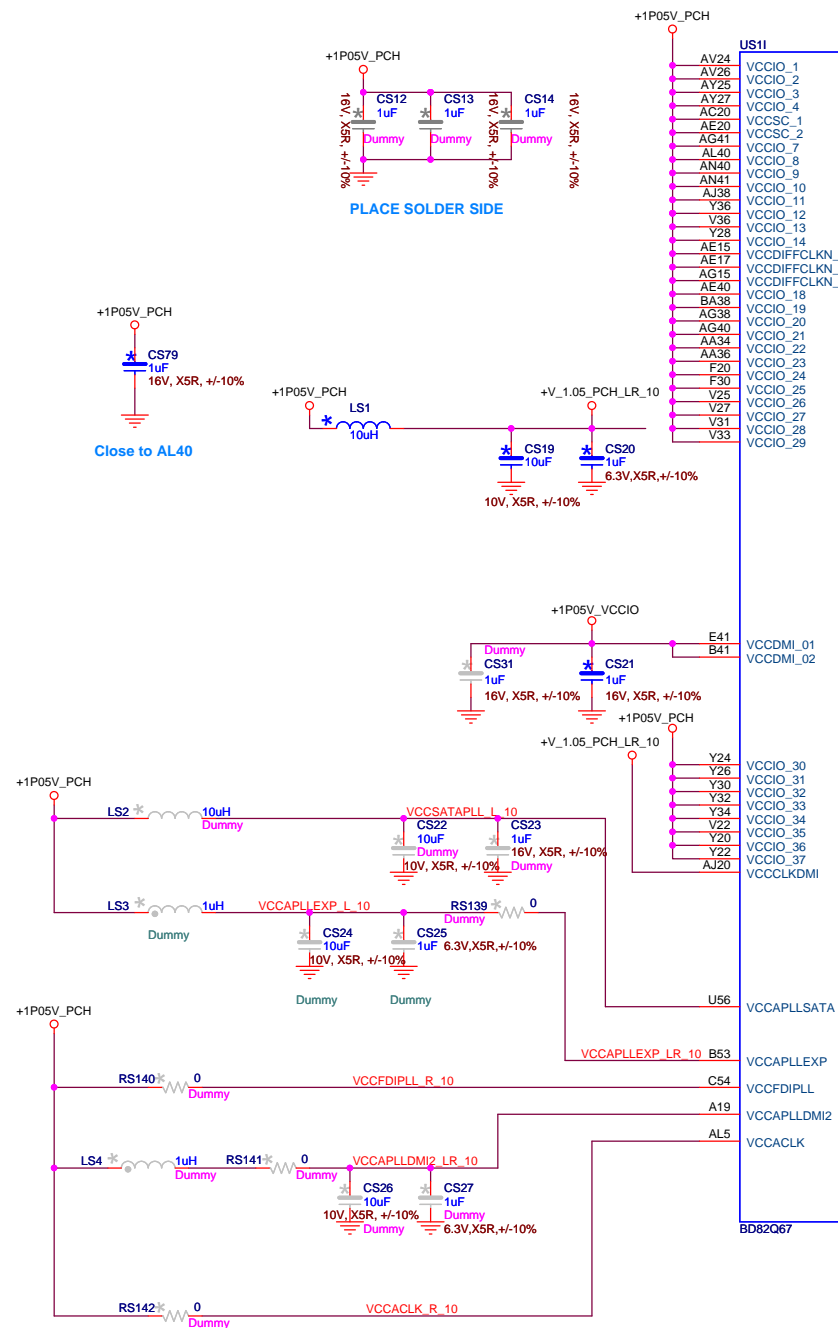


20091216 PCIECLKRQ1#/GPIO18 is mobile chip only, RC110, RC111 and signal net "S_PCIECLKREQ#1" removed.

20100106: GPO_WLOM move to GPIO14

Pull-down for Integrated clock gen-11/25/09
 20100105: Dummy all pull-down resistors since use buffer thru mode
 20100106: Reserved RC123,RC124; CRB 0.7
 20100107: RC121,RC122 mount; PDG 0.8

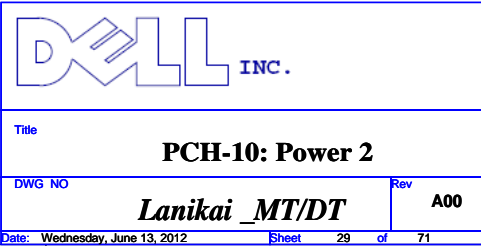




D25	USB3Tp4
B27	USB3Tp3
E27	USB3Tp2
E29	USB3Tp1
B25	USB3Tn4
C26	USB3Tn3
F28	USB3Tn2
C29	USB3Tn1
J22	USB3Rp4
L25	USB3Rp3
L27	USB3Rp2
J31	USB3Rp1
L22	USB3Rn4
J25	USB3Rn3
J27	USB3Rn2
H31	USB3Rn1

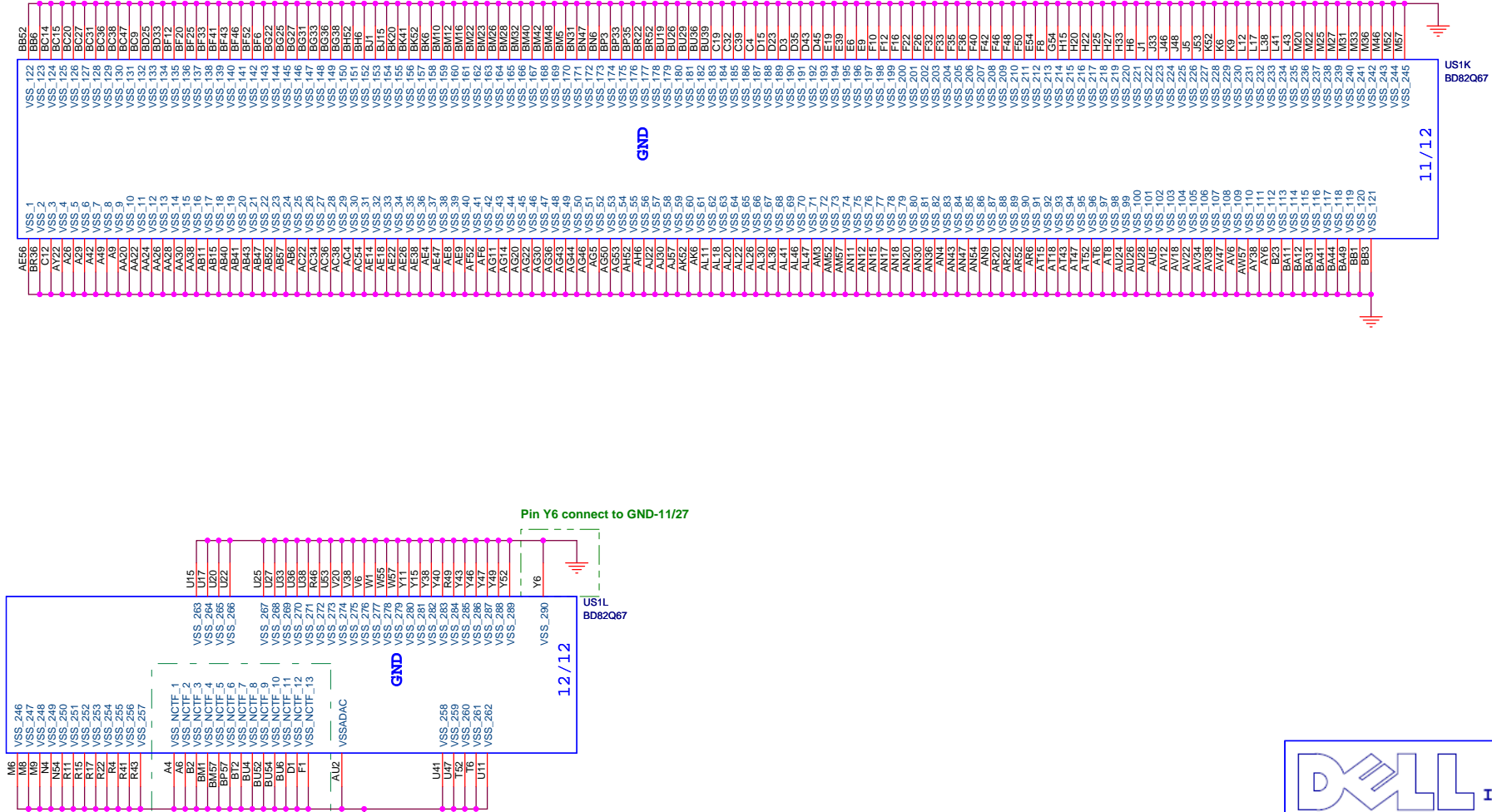
Intel

PCH-9: Power 1



~~By Dell request remove US1_1 PCH heatsink detect for RTCSRST net spacing~~

~~By Dell request remove US1_1 PCH heatsink detect for RTCSRST net spacing~~



Title

PCH-11: GND

DWG NO

Lanikai MT/DT

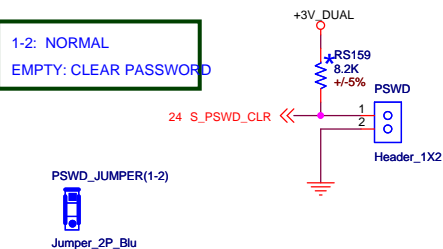
Rev

A00

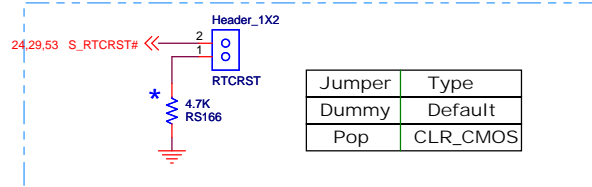
Date: Wednesday, June 13, 2012

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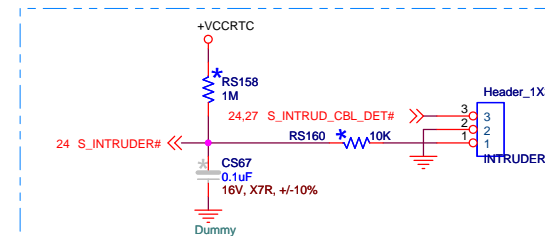
Clear Password



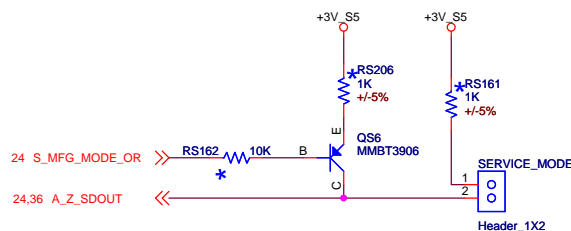
CLR_CMOS



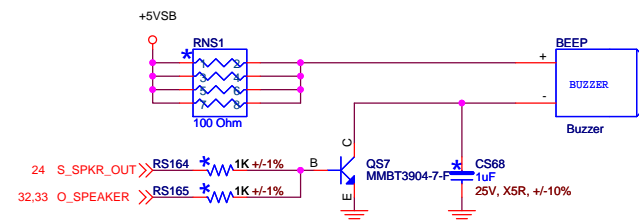
Chassis Intruder



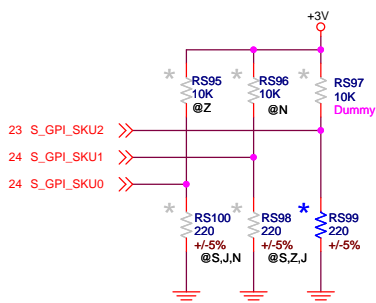
SERVICE_MODE



BEEP



SKU ID



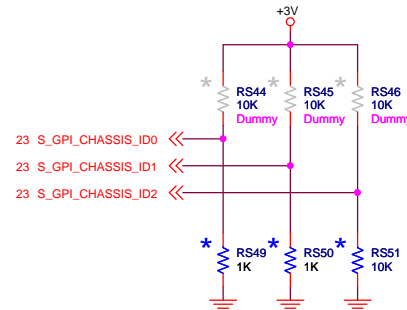
SKU ID

SKU1	SKU0	Type
0	0	TPM
0	1	TCM
1	0	non TPM/TCM
1	1	Reserved

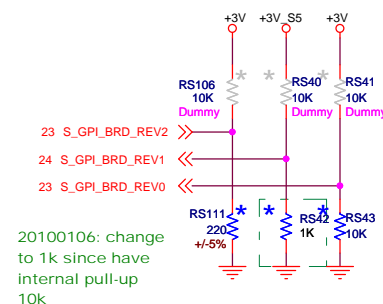
Chassis ID

check : need to update table

ID2	ID1	ID0	Type
1	0	1	SFF
1	0	0	Comoros
0	0	0	MT/DT
0	1	1	USFF

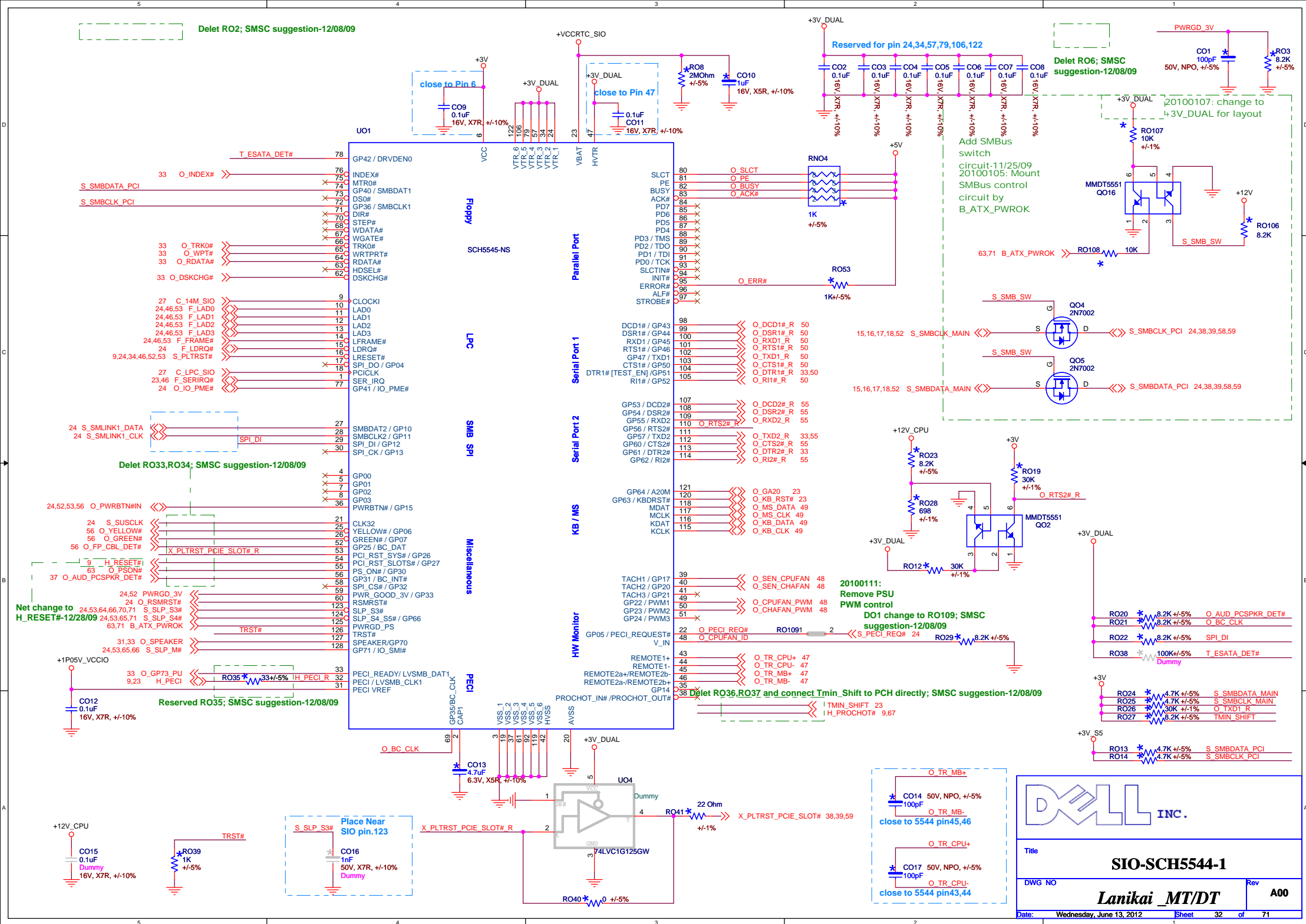


BOARD ID

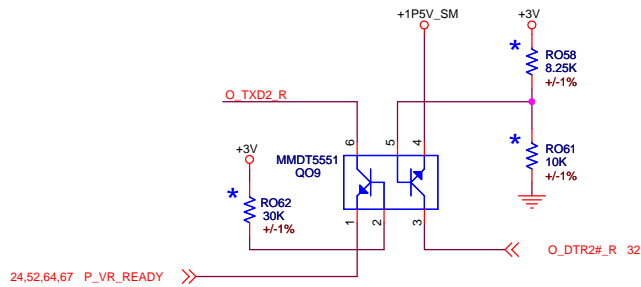
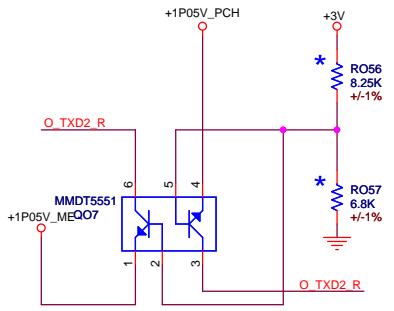
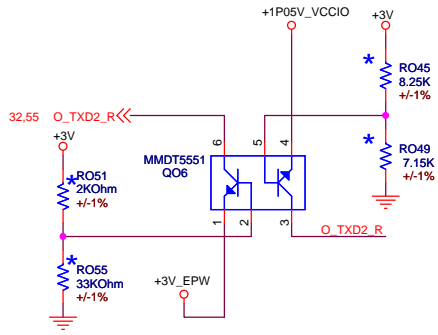
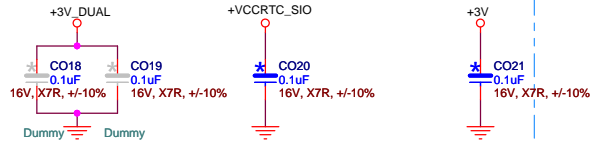


Rev2	Rev1	Rev0	Type
0	0	0	Default
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

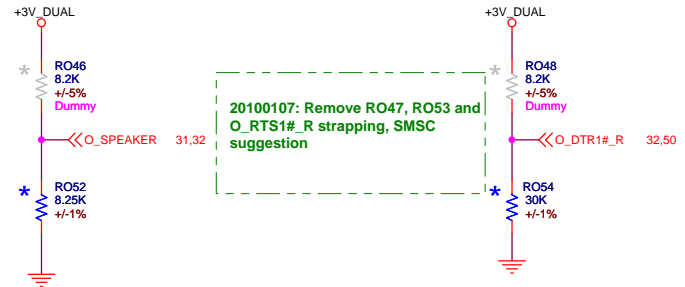




SCH5544 Decoupling

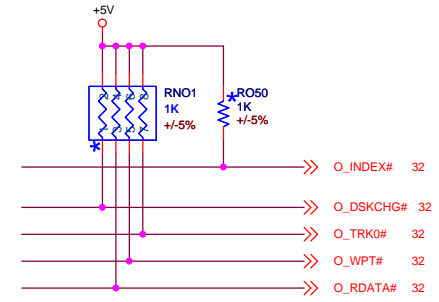
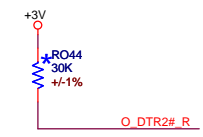
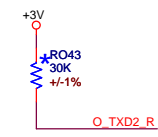
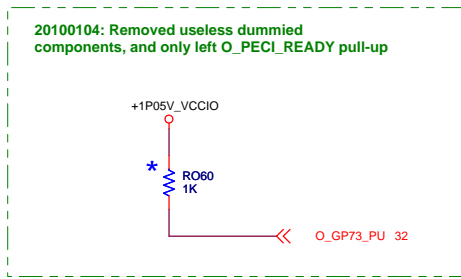


5544 PRE-POST DIAG PG GENERATION



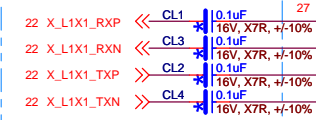
	SPEAKER	DTR1#
	Diag_En	Flash_en
PULL HIGH	Disable	Flash Enable
PULL LOW	Enable	Parallel Enable

SIO STRAPING



20091216 Intel 82579 schematic check list 0.5:
Change net name from CLK_REQ_N to S_FLEXBAY_HDR_CBL_DET#
20100105: Remove RL2 and S_FLEXBAY_HDR_CBL_DET#
connection since useless; PDG 0.8

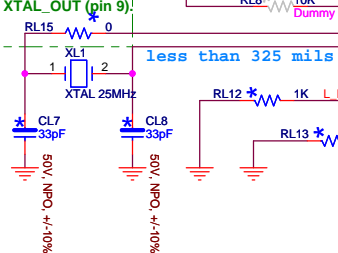
near the PCIe transmitter.



24 S_SMLINK0_CLK
24 S_SMLINK0_DATA

L LAN_DISABLE#

20091216 CRB0.7 :Connect a series CL24
(10 pF) capacitor to XTAL_OUT (pin 9)!

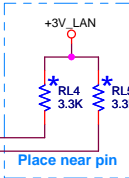


L LAN_TESTEN

TEST_ENABLE

RBIAS

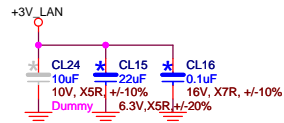
21040FE00-187-G



Place close to PHY



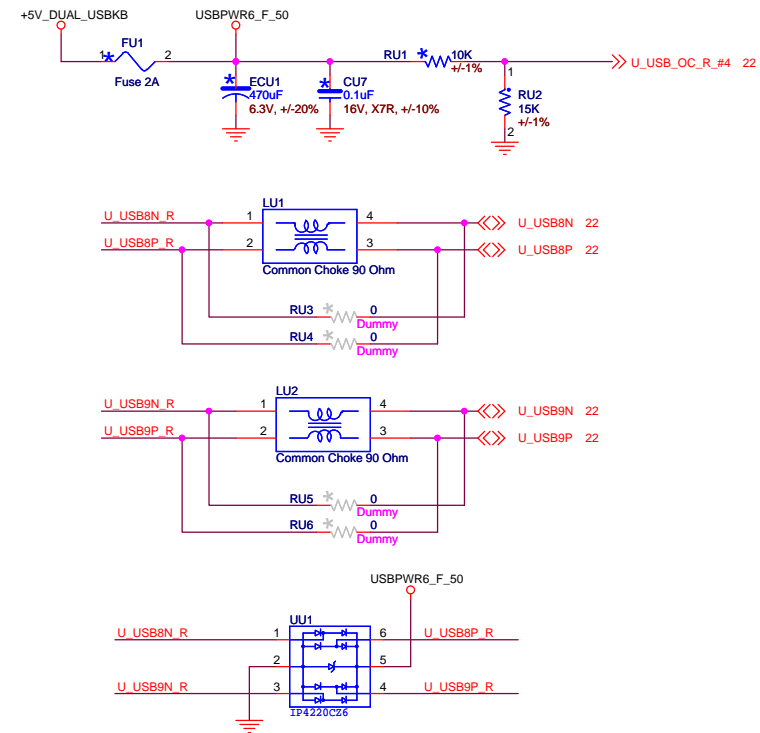
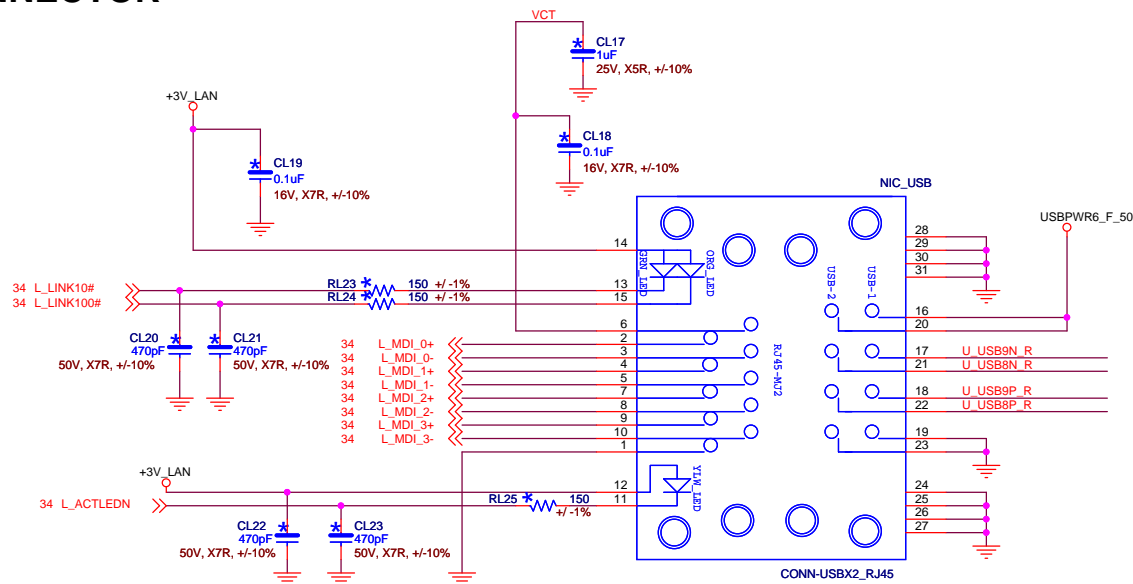
Close to PIN5 (VDD)



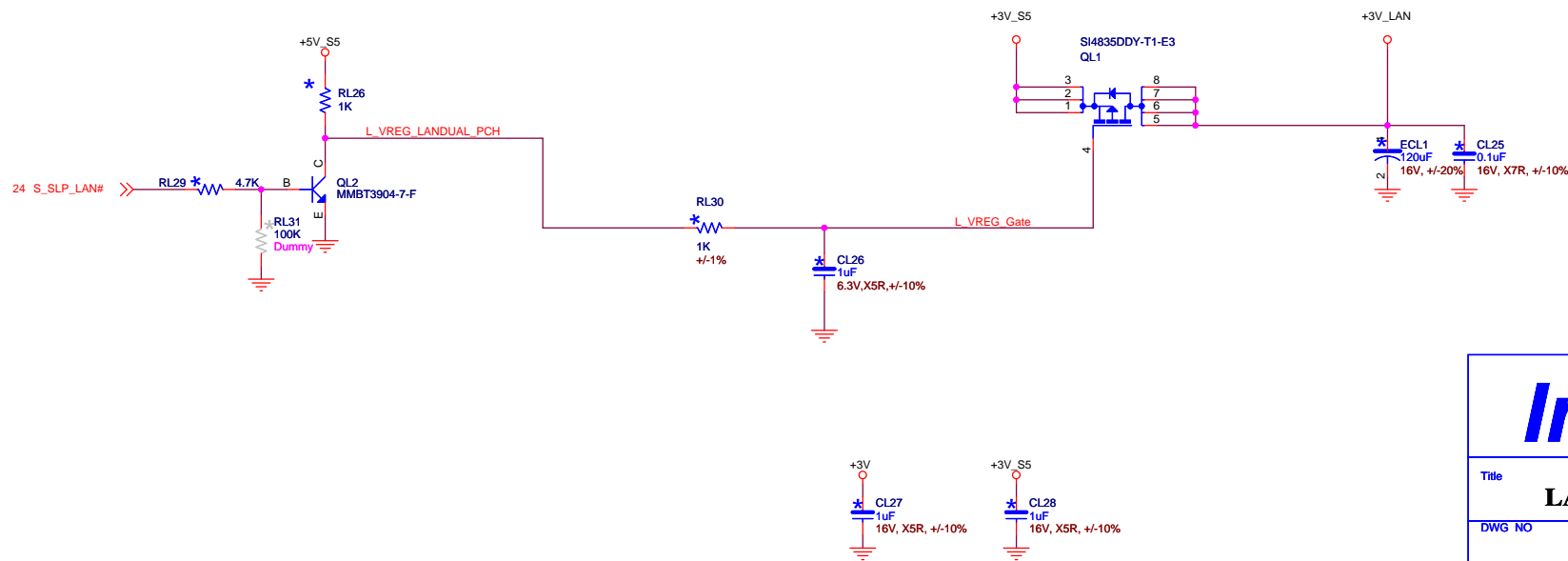
20091216 follow CRB0.7 and 82579 checklist: does not require any MDI termination.(delete => RL15, RL16, RL17, RL18, RL19, RL20, RL21, RL22, CL11, CL12, CL13, CL14)



LAN CONNECTOR



LAN POWER



Title

LAN Power & LAN/USB Conn

DWG NO

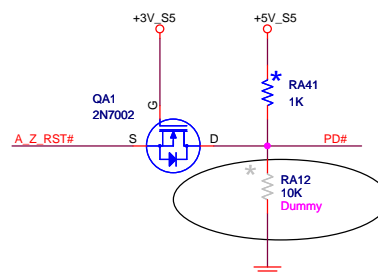
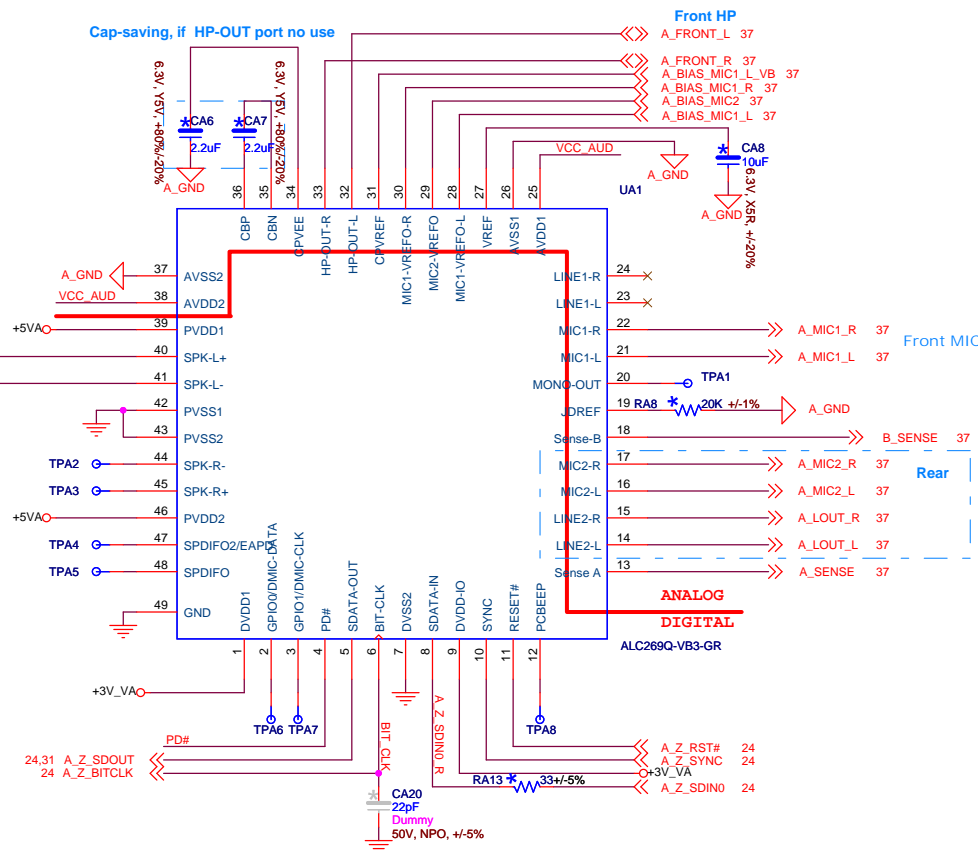
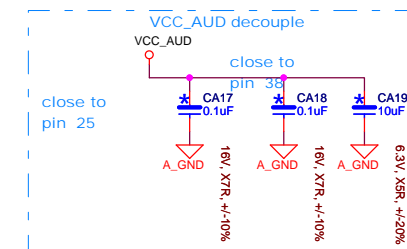
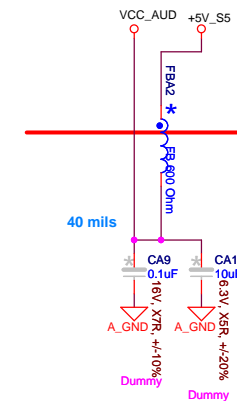
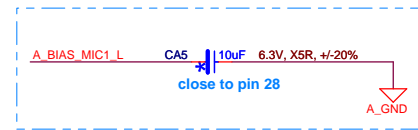
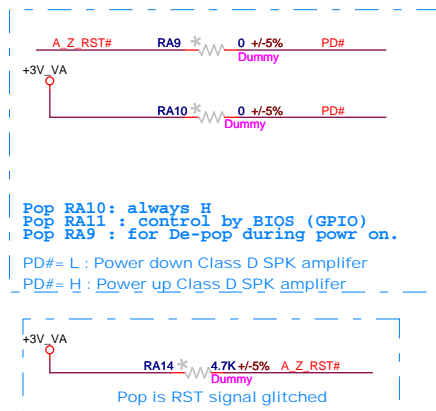
Lanikai_MT/DT

Date: Wednesday, June 13, 2012

Rev

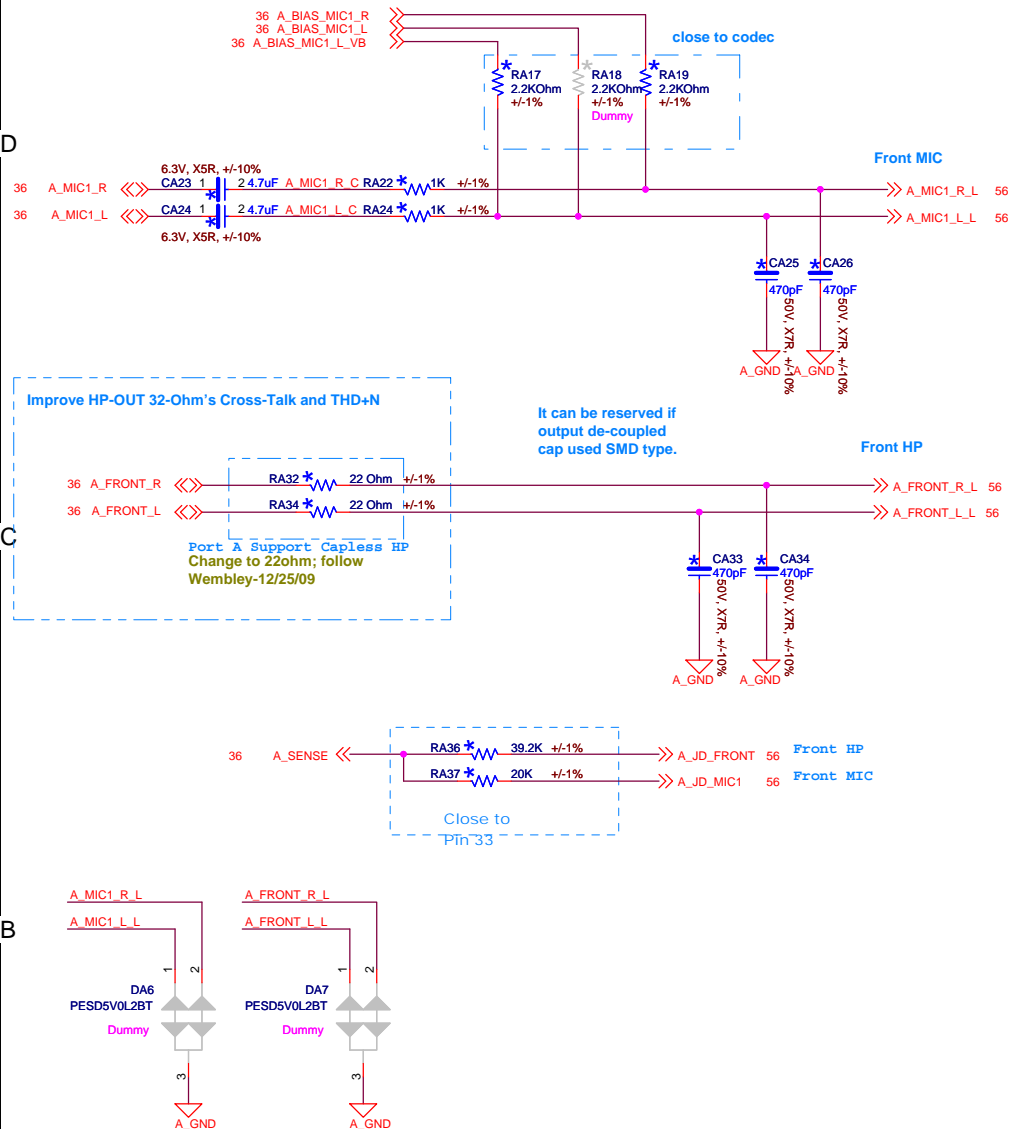
A00

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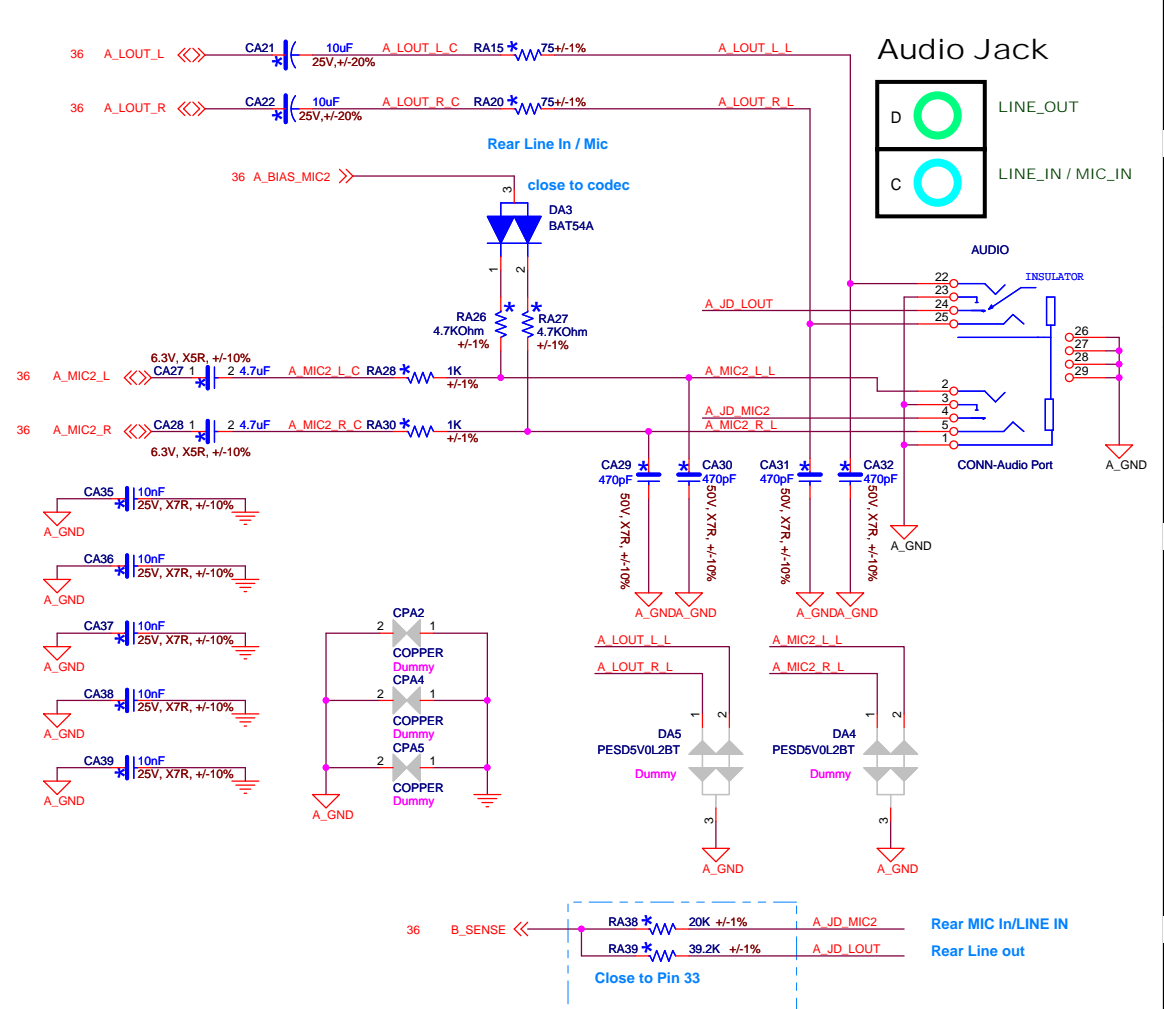


RA12 reserved for co-layout ALC269-VC

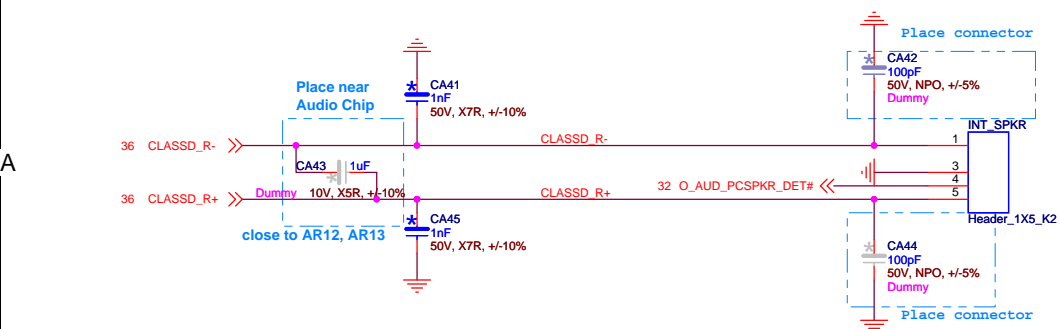
Front Audio



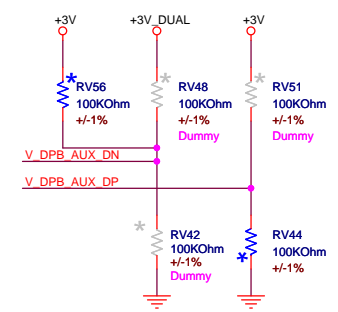
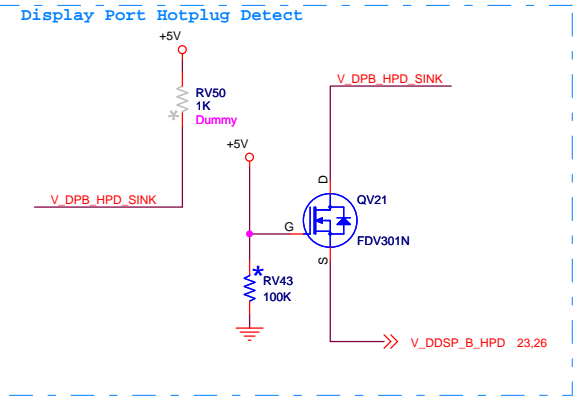
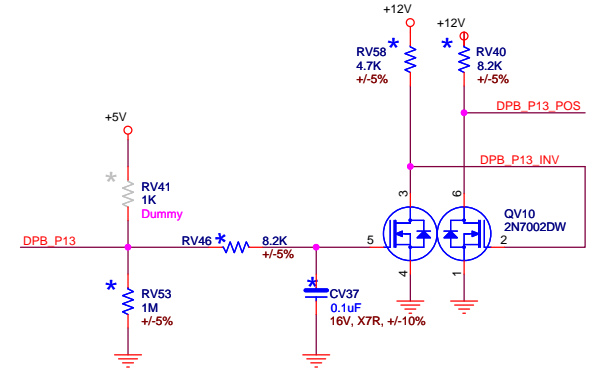
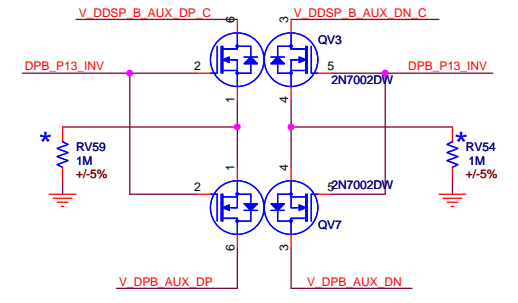
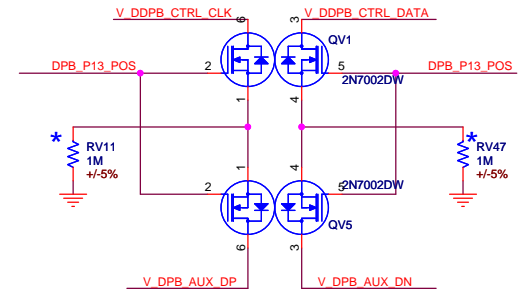
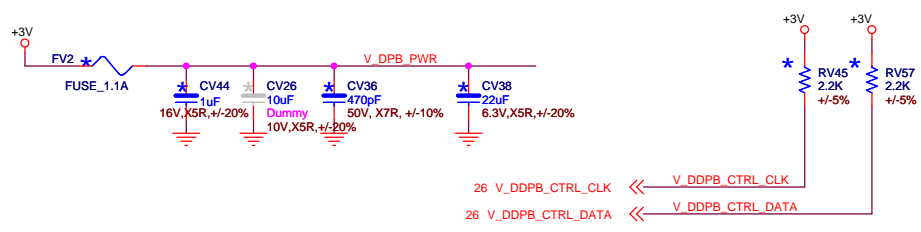
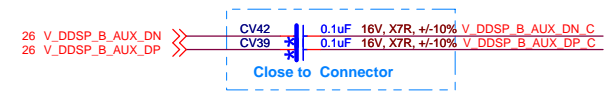
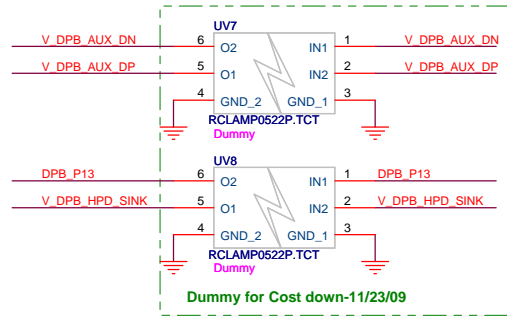
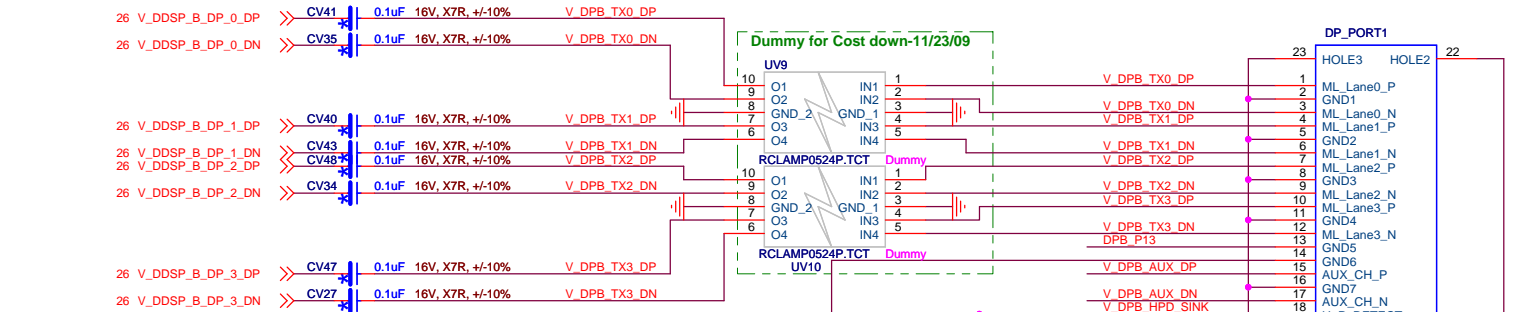
Rear Audio Jack




CHASSIS SPEAKER



DELL INC.	
Title	
Audio Conn	
DWG NO	Rev
Lanikai_MT/DT	A00
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INC.

Title

DVI-D+VGA Conn

DWG NO

Lanikai_MT/DT

Rev

A00

Date:

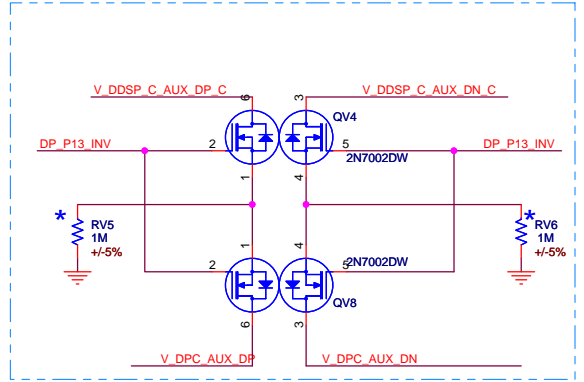
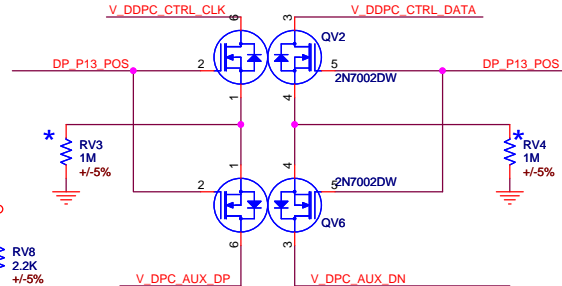
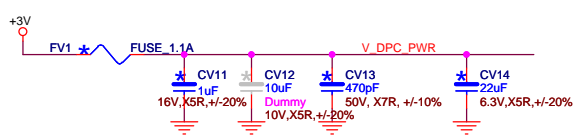
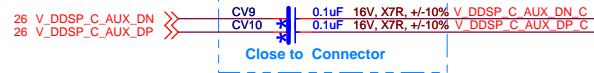
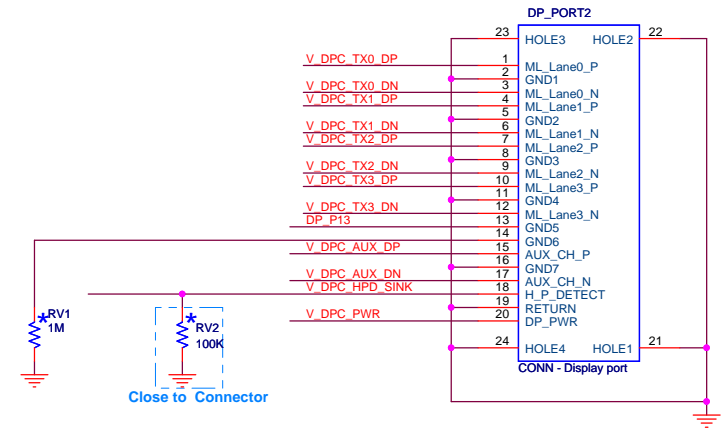
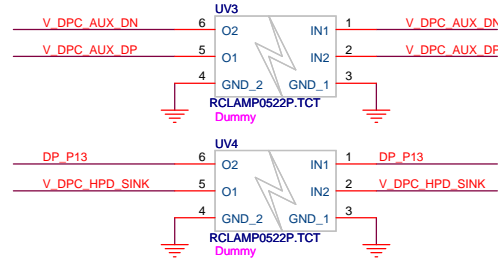
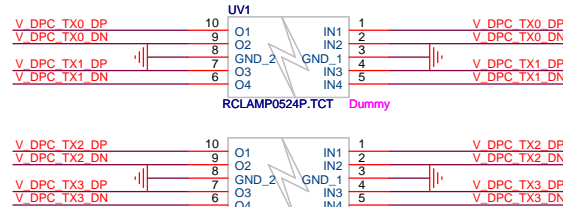
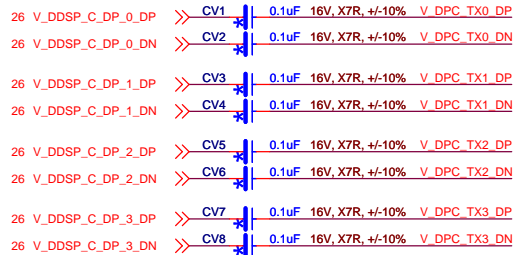
Wednesday, June 13, 2012

Sheet

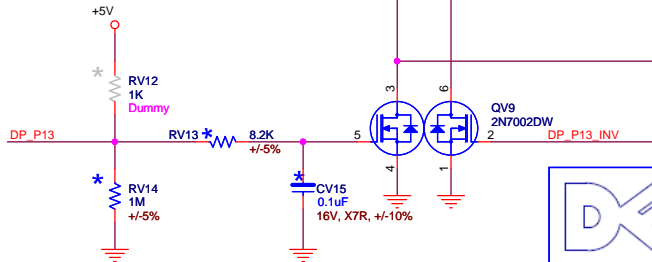
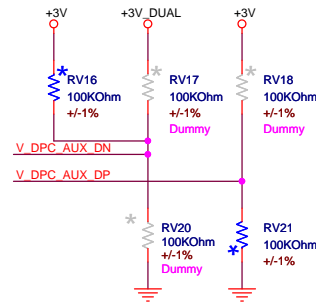
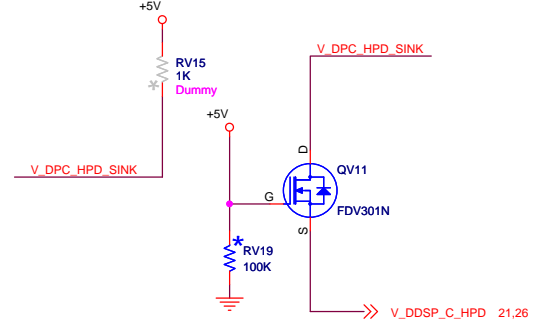
40

of

71



Display Port Hotplug Detect



DELL INC.

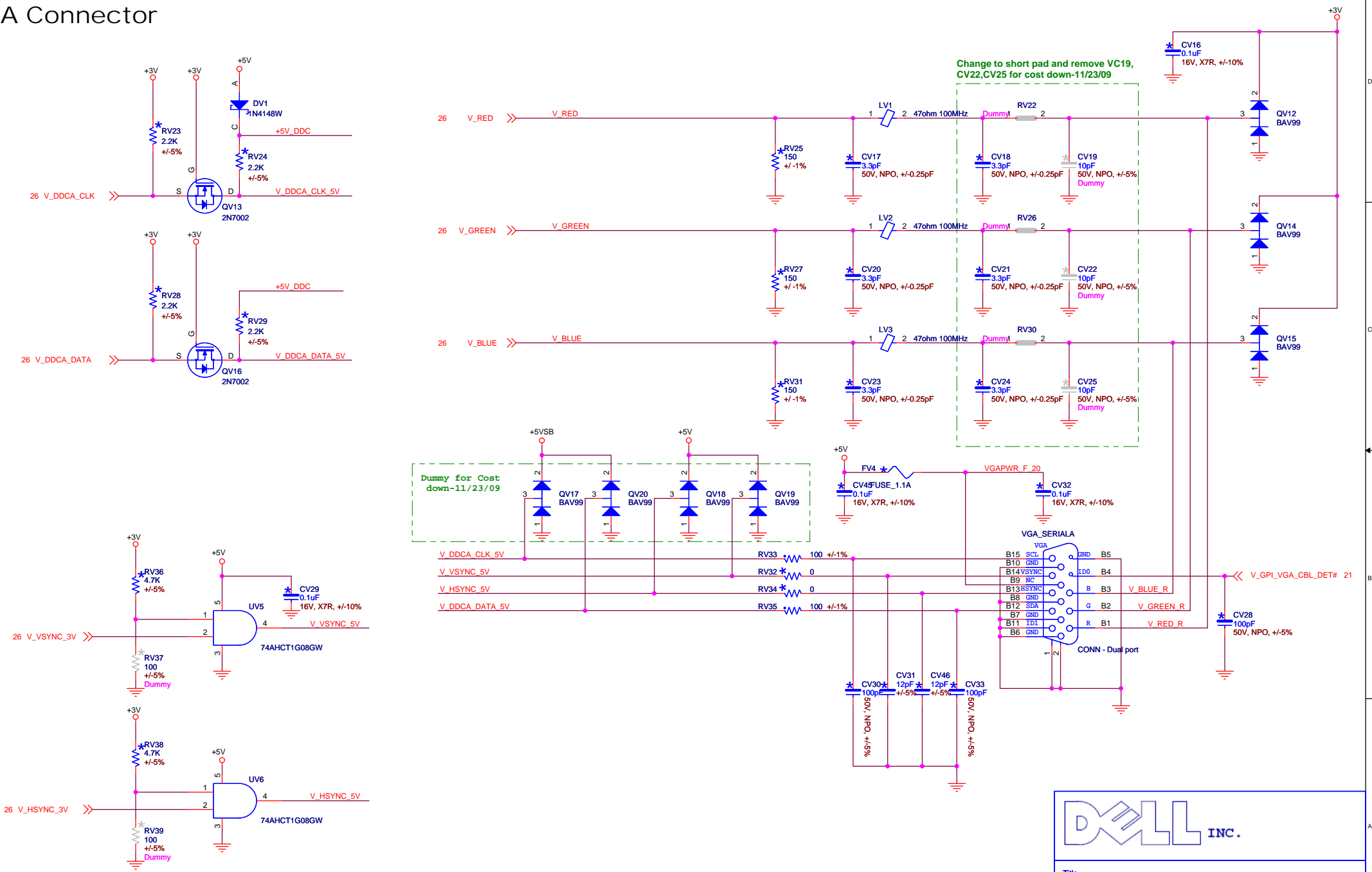
Title
Display Port

DWG NO
Lanikai_MT/DT

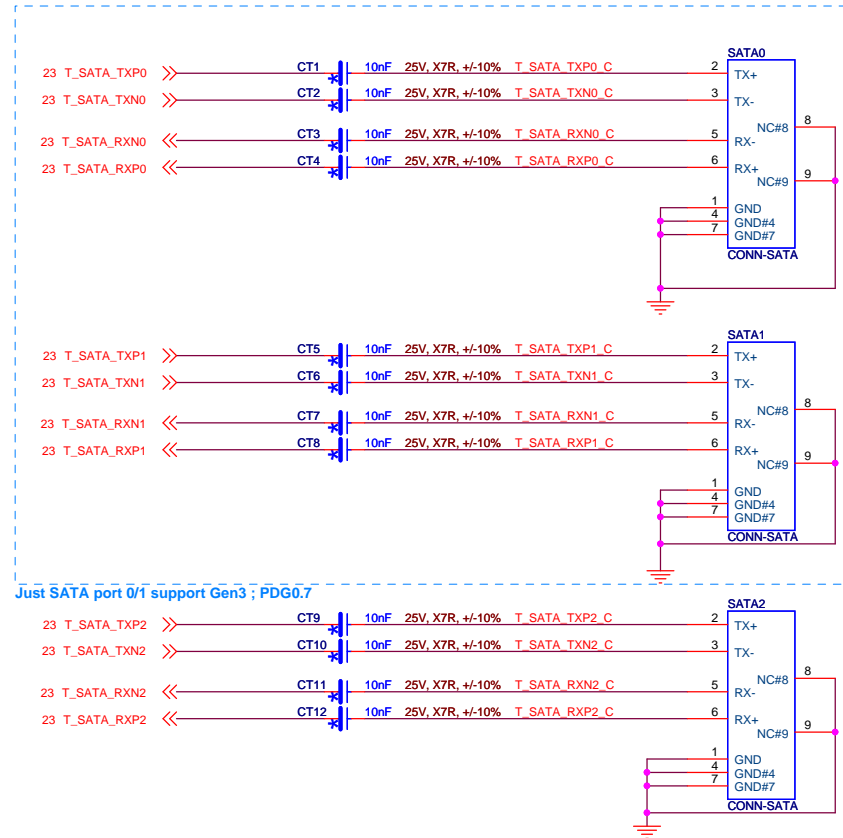
Rev
A00

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VGA Connector

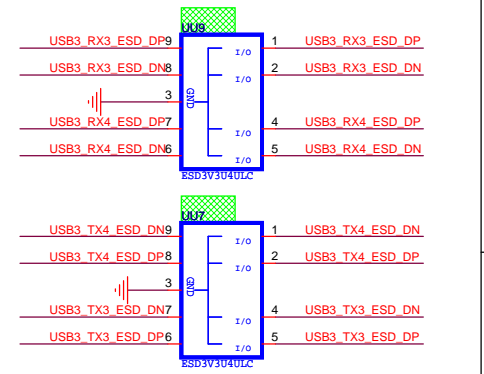
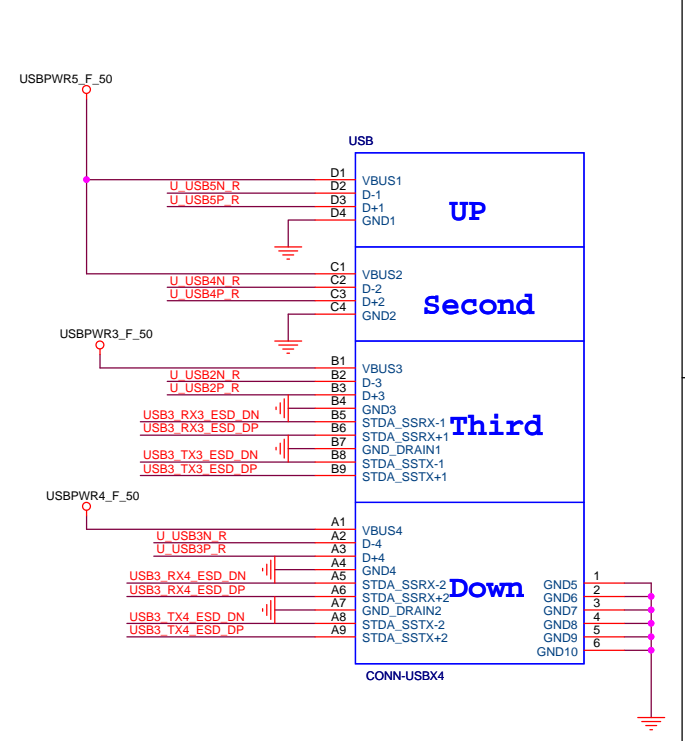
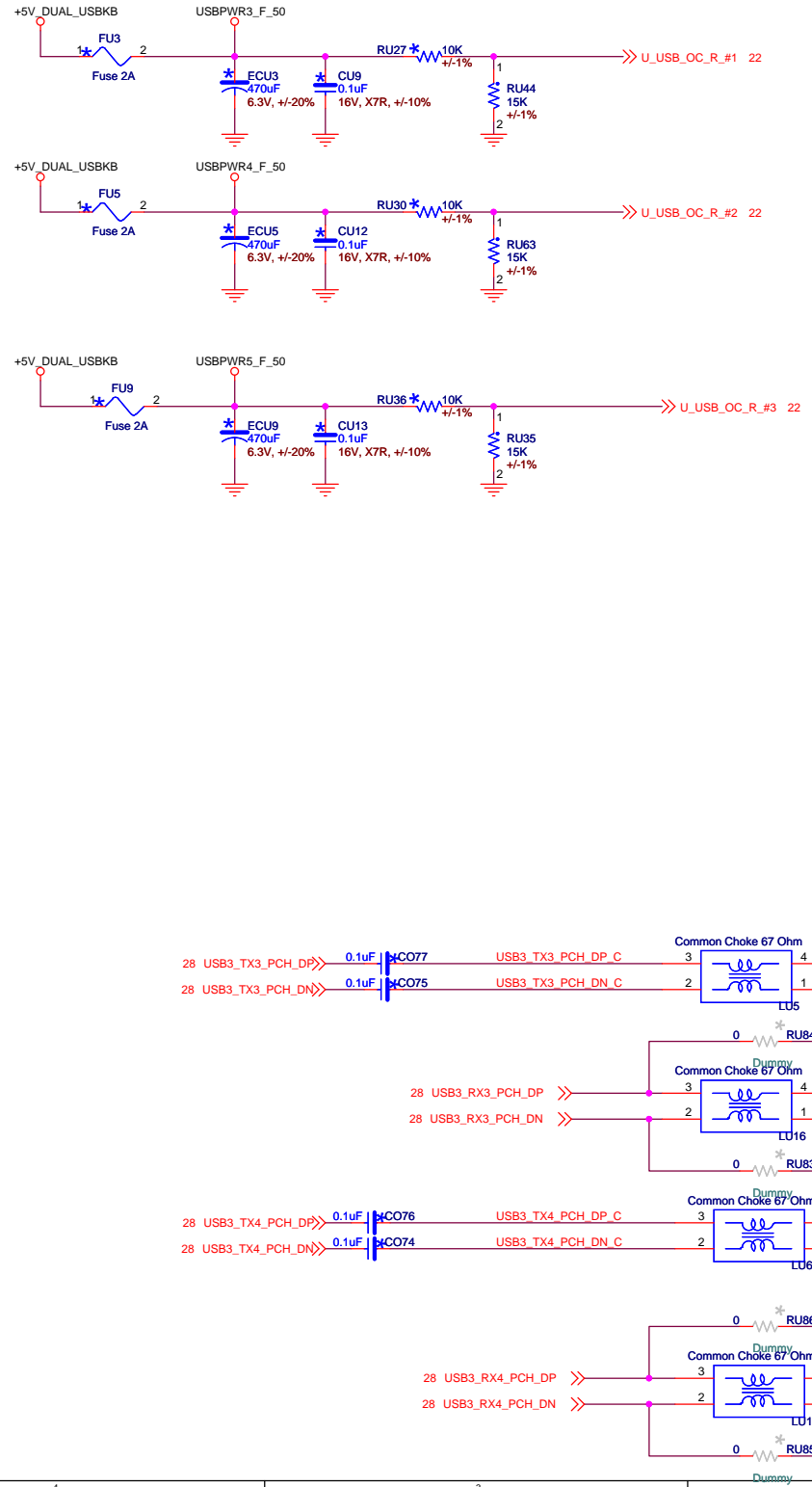
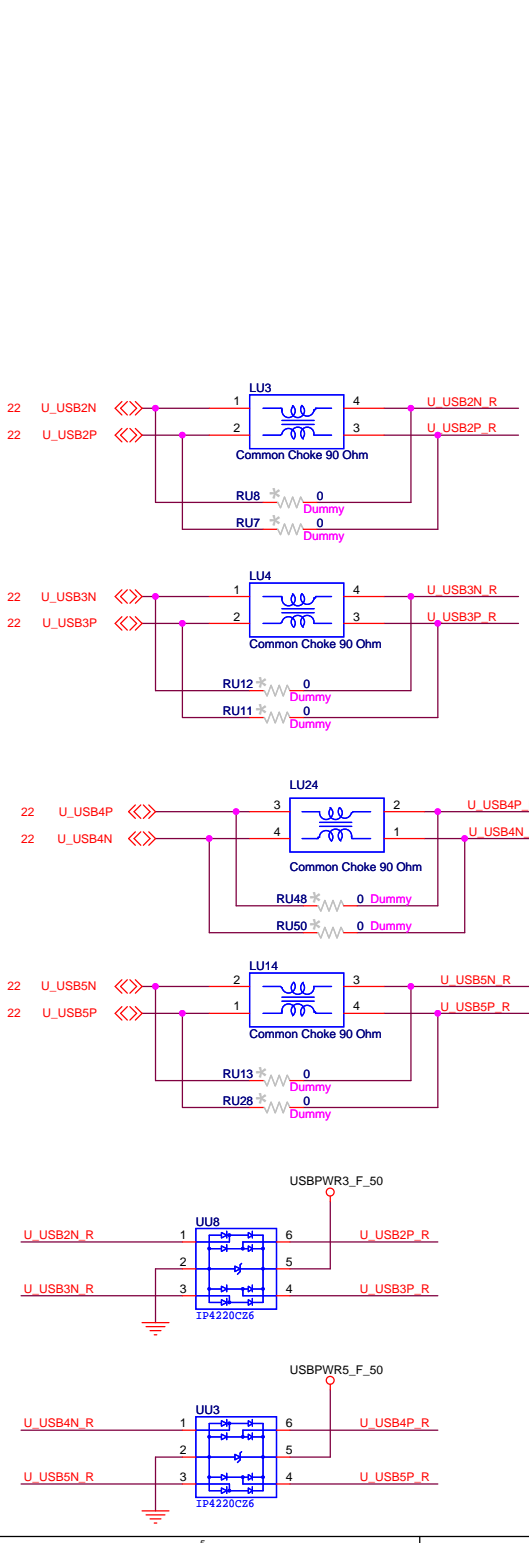


SATA x 3





 INC.	
Title TBD	
DWG NO	Rev A00
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Intel

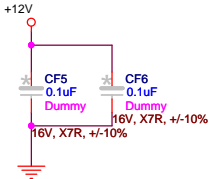
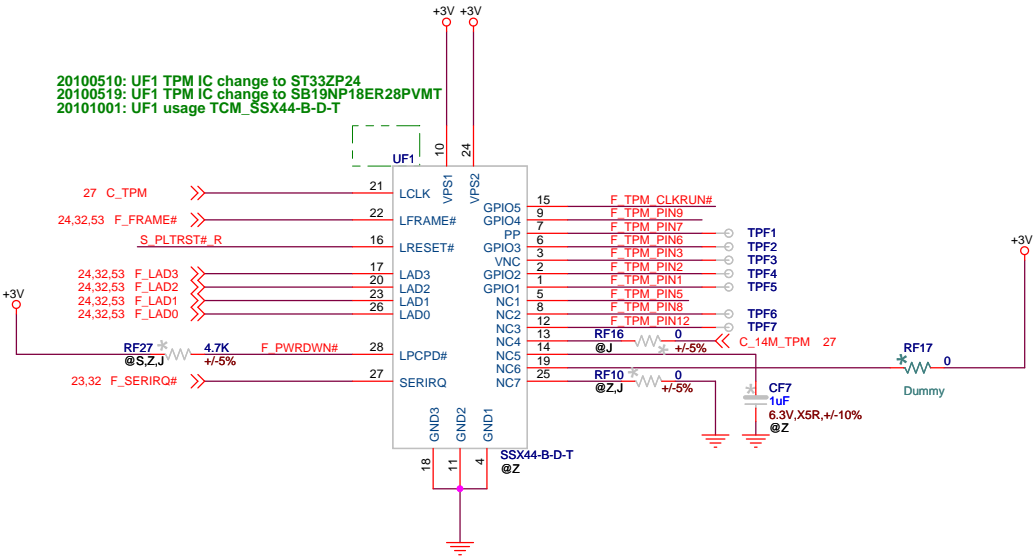
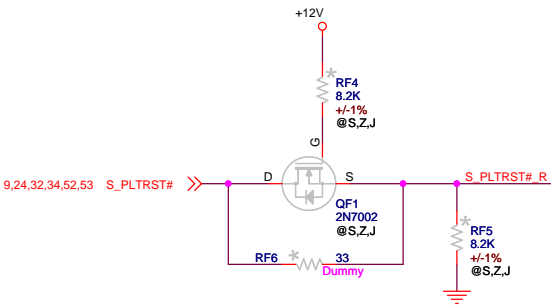
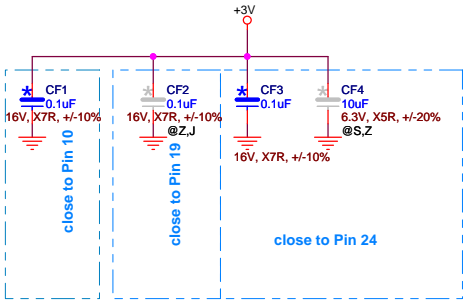
Rear USB

DWG NO **Lanikai_MT/DT** Rev **A00**

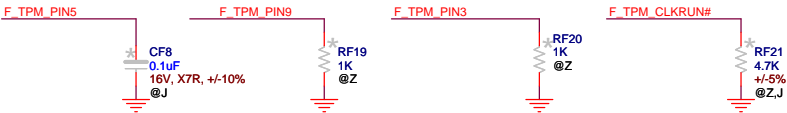
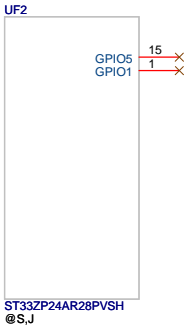
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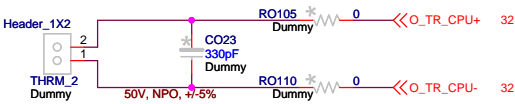
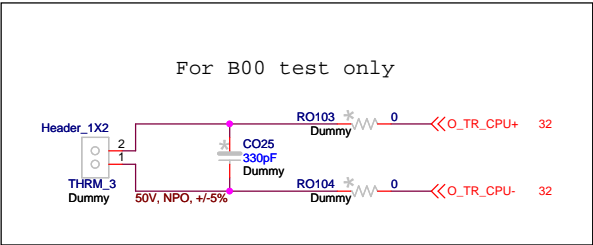
TPM, TCM (TCM is just reserved because MRD has removed TCM requirement)

(Default) ST Micro	POP S	CF4
ZTE	POP Z	CF2,CF4,CF7,RF10,RF19,RF20,RF21
Jetway	POP J	CF2,CF8,RF10,RF16,RF21

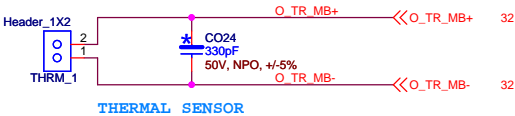


20101001: add UF2 usage TPM_SB19NP18ER28PVMK

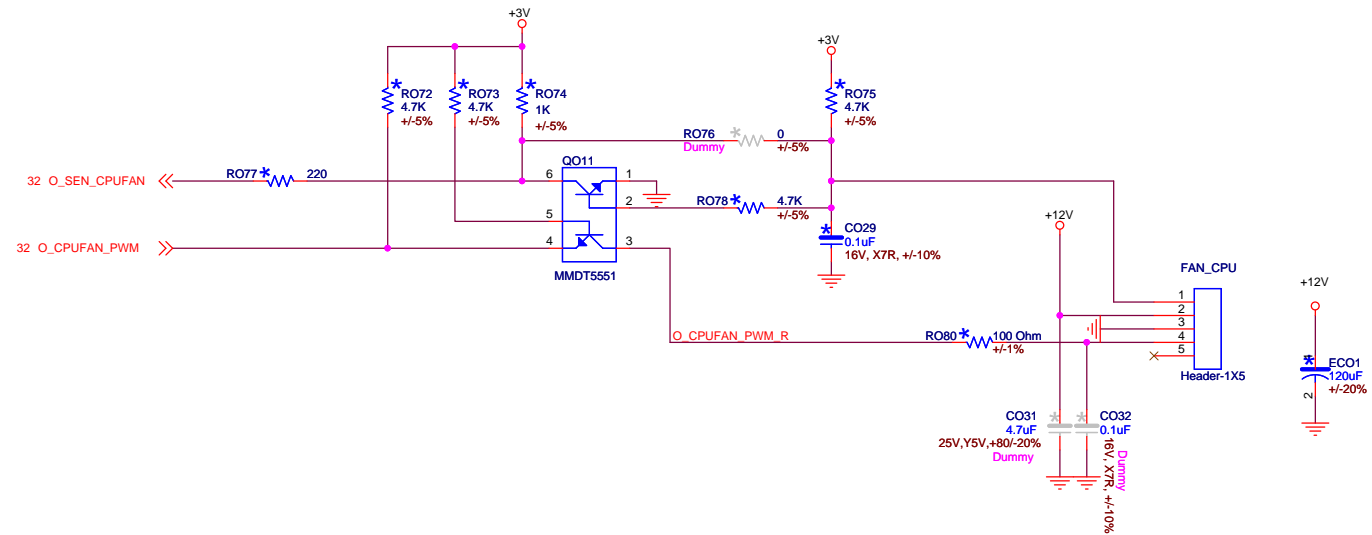




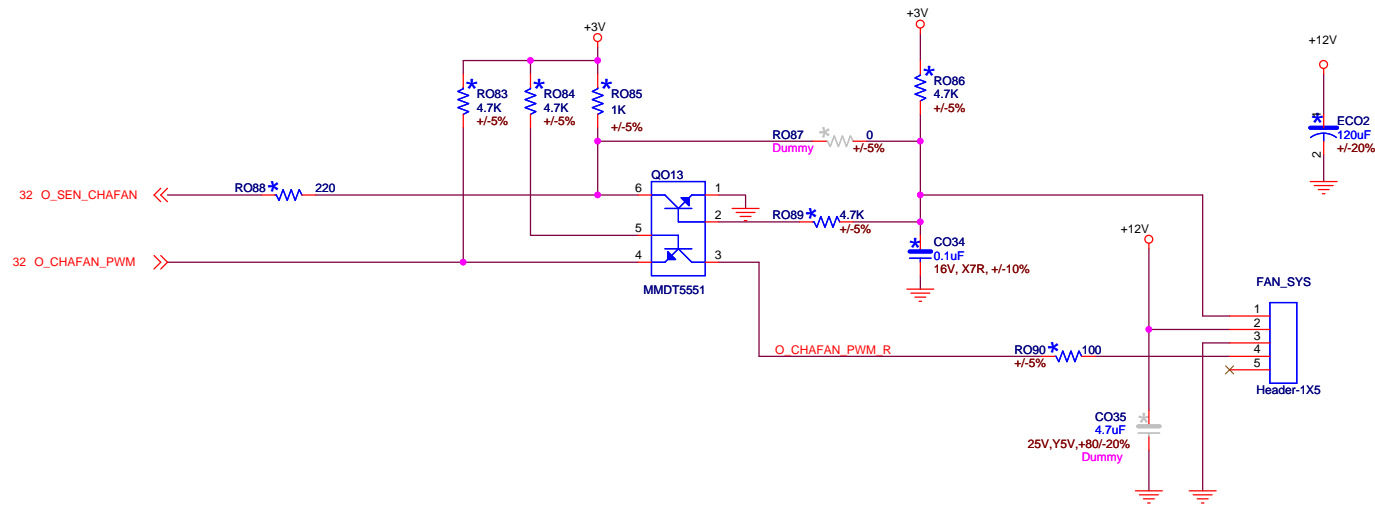
Dummy THRM2,CO23; ME suggestion-12/04/09



CPU Fan



SYS Fan



Title

FAN

DWG NO	
--------	--

Lanikai_MT/DT

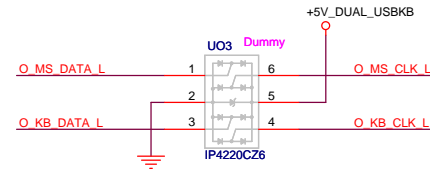
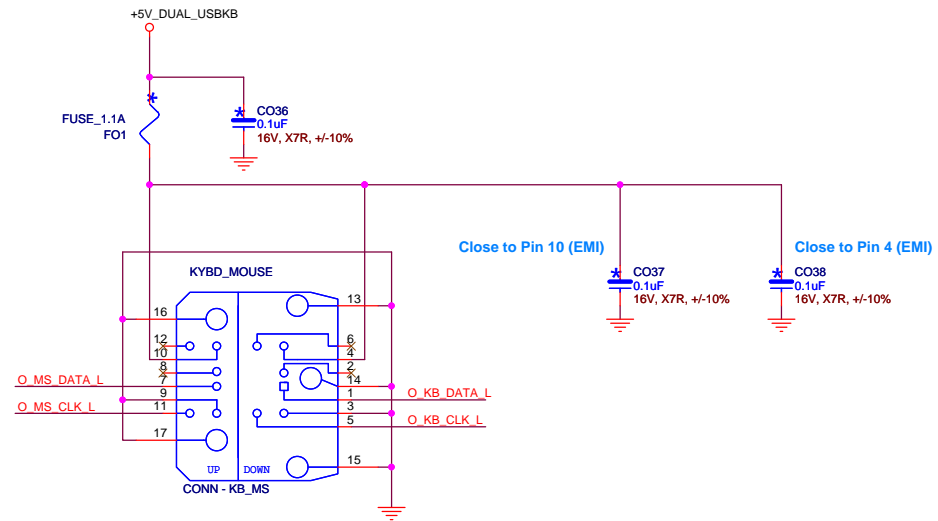
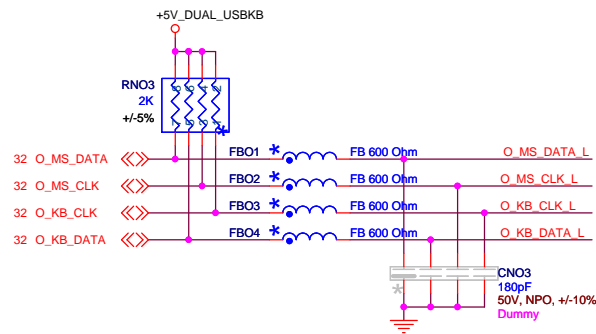
Rev

A00

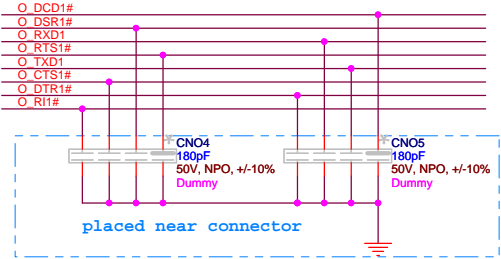
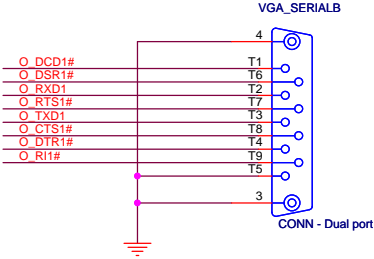
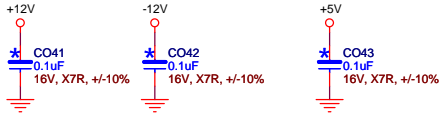
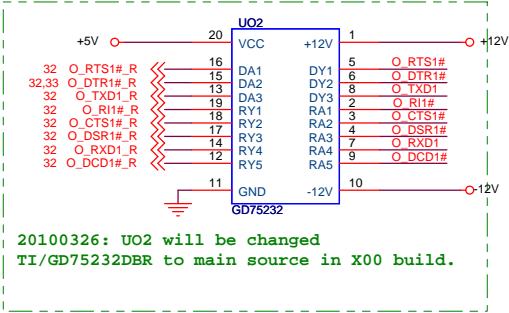
Date: Wednesday, June 13, 2012

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KB/MS

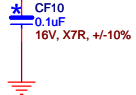
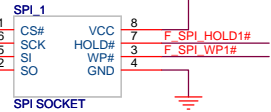
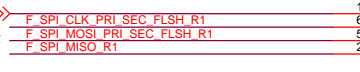


Serial Port 1

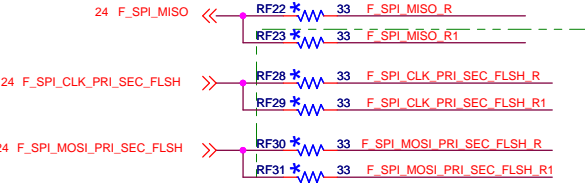


SPI

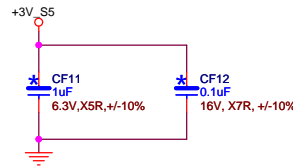
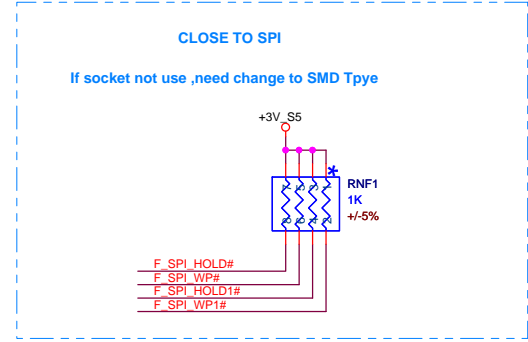
24 F_SPI_CS1#_ISOLATE >>
20091225: Change net name for Dual SPI



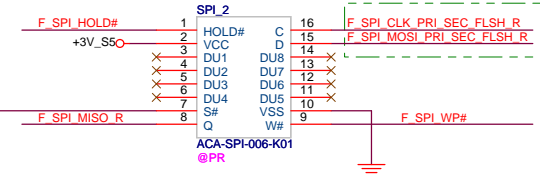
20110530: Change to 4M



20091225: RF23 change to 33ohm for Dual SPI
20091225: Add RF28, RF29, RF30, RF31 for Dual SPI

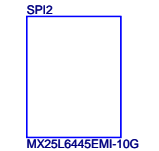


24 F_SPI_CS0#_ISOLATE >>

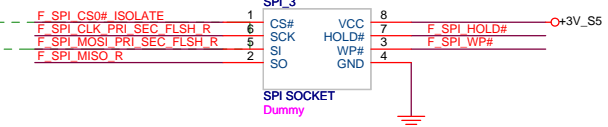


20091225: Change net name for Dual SPI

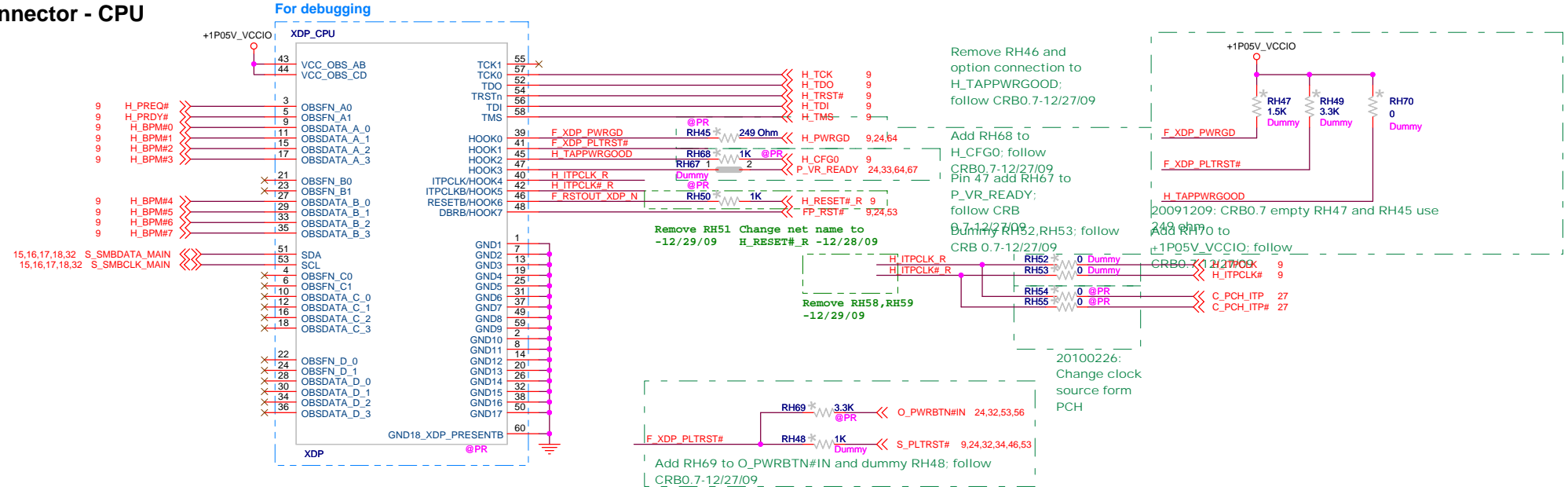
20100309: SPI2 Package Type change to DIP from SMD, when usage SPI_2 socket
20100930: SPI2 change to MXIC_MX25L6445EMI-10G



20091225: Change net name for Dual SPI

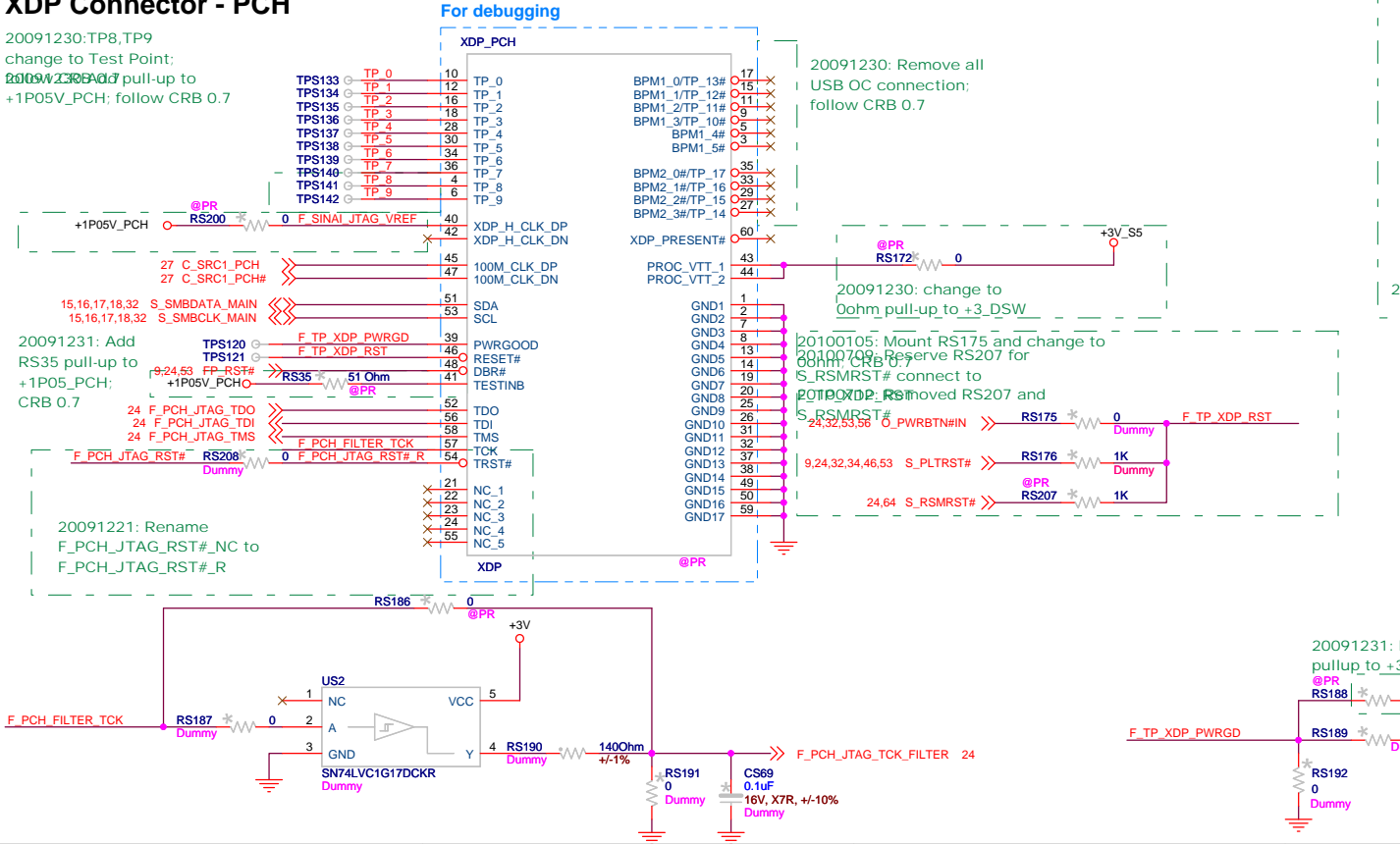


XDP Connector - CPU



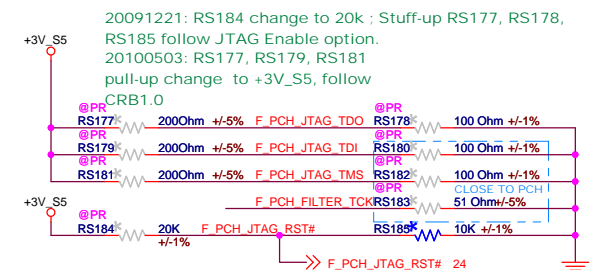
XDP Connector - PCH

20091230:TP8,TP9
change to Test Point;
2010W2CRB Add pull-up to
+1P05V_PCH; follow CRB 0.7



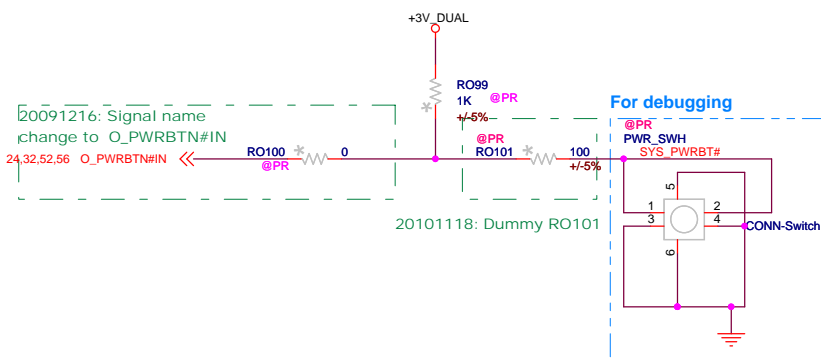
2009/12/21 Update JTAG Table		PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
F_PCH_JTAG_TDO	RS177	No Stff	200 Ohms ¹	No Stuff	No Stuff
	RS178	No Stff	100 Ohms ¹	No Stuff	No Stuff
F_PCH_JTAG_TMS	RS179	200 Ohms	200 Ohms	No Stuff	No Stuff
	RS180	100 Ohms	100 Ohms	No Stuff	No Stuff
F_PCH_JTAG_TDI	RS181	200 Ohms	200 Ohms	20K Ohms	No Stuff
	RS182	100 Ohms	100 Ohms	10K Ohms	No Stuff
F_PCH_FILTER_TCK	RS183	51 Ohms	51 Ohms	51 Ohms	51 Ohms
F_PCH_JTAG_RST#	RS184	20K Ohms	20K Ohms	No Stuff	No Stuff
	RS185	10K Ohms	10K Ohms	No Stuff	No Stuff

20091221: updated JTAG stuffing table

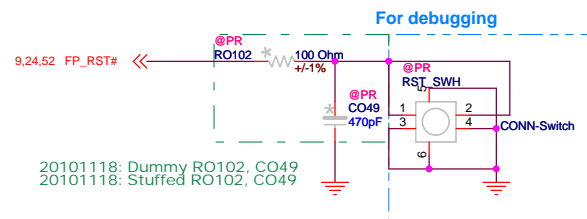


Title			
XDP			
DWG NO			Rev
<i>Lanikai_MT/DT</i>			A00
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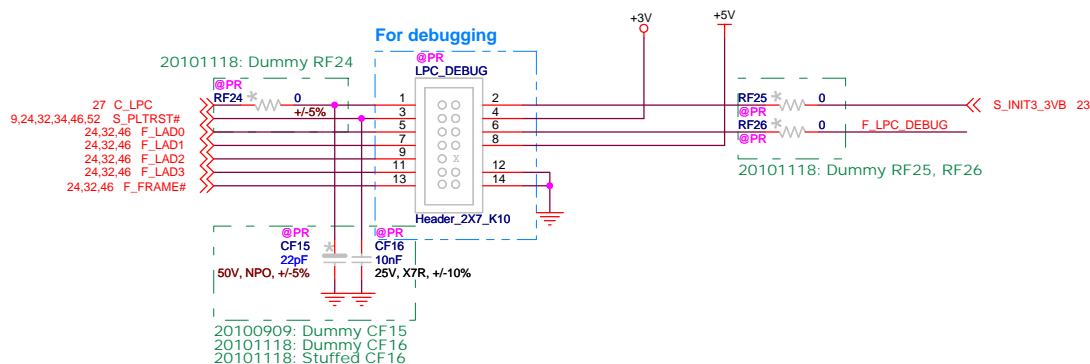
Power Bottom



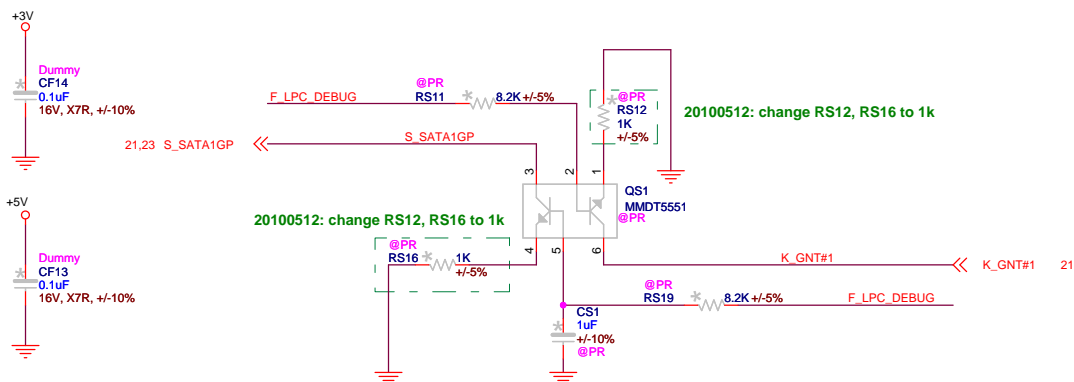
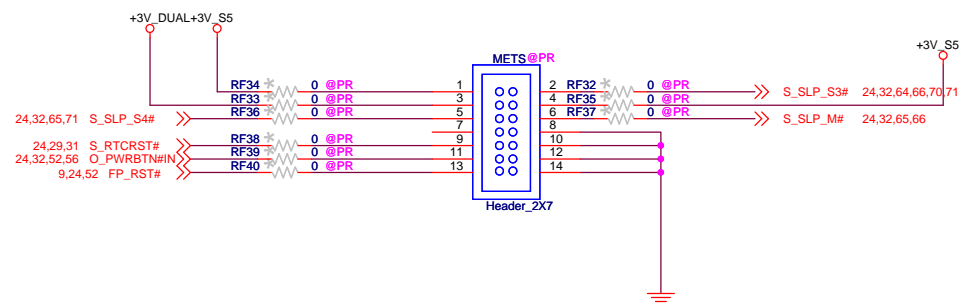
Reset Bottom



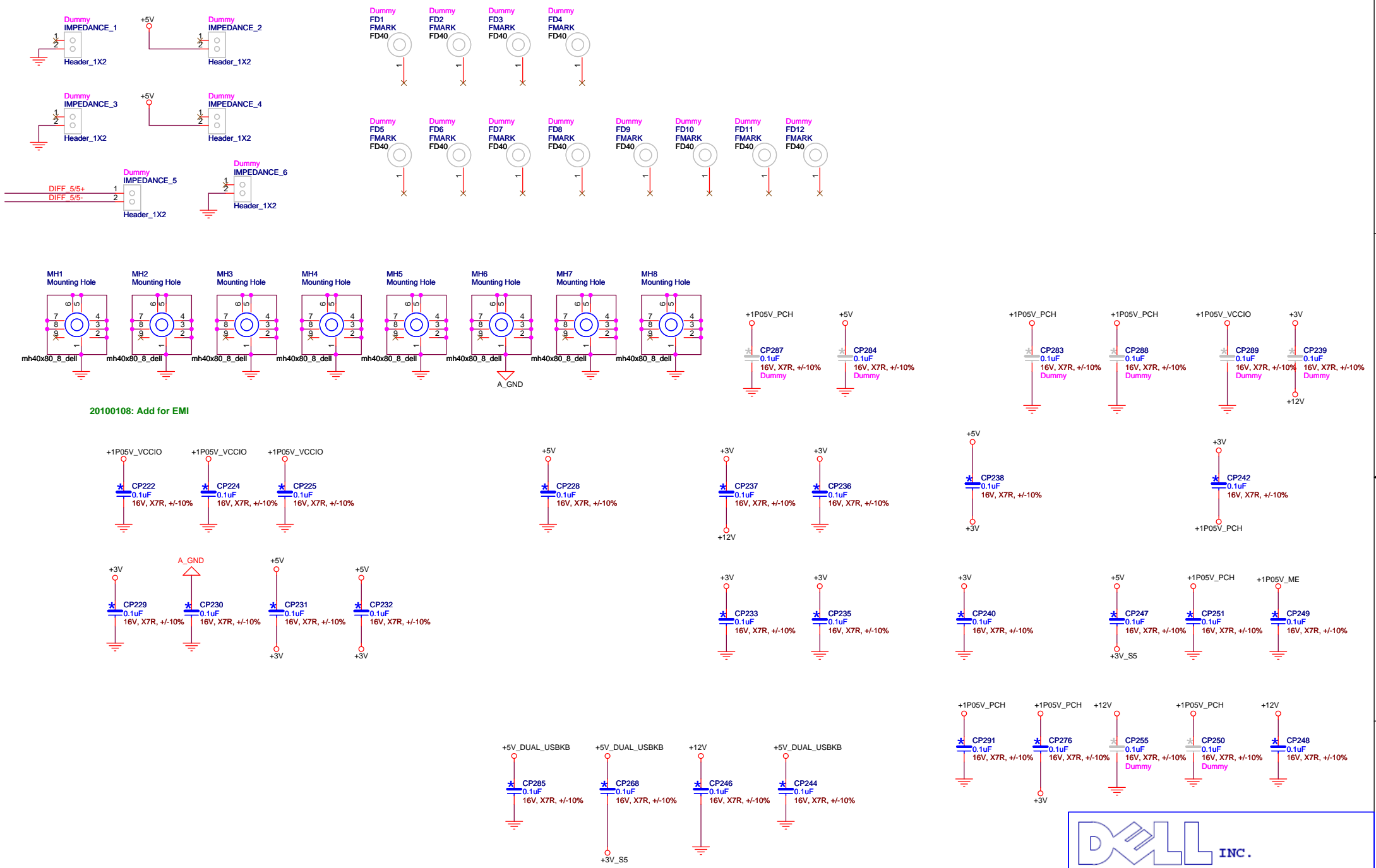
LPC DEBUG




APS Connector



		INC.	
Title			
Pilot Run Conn			
DWG NO		Rev	
Lanikai_MT/DT		A00	
Date:	Wednesday, June 13, 2012	Sheet	53 of 71

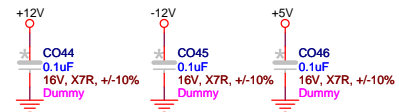
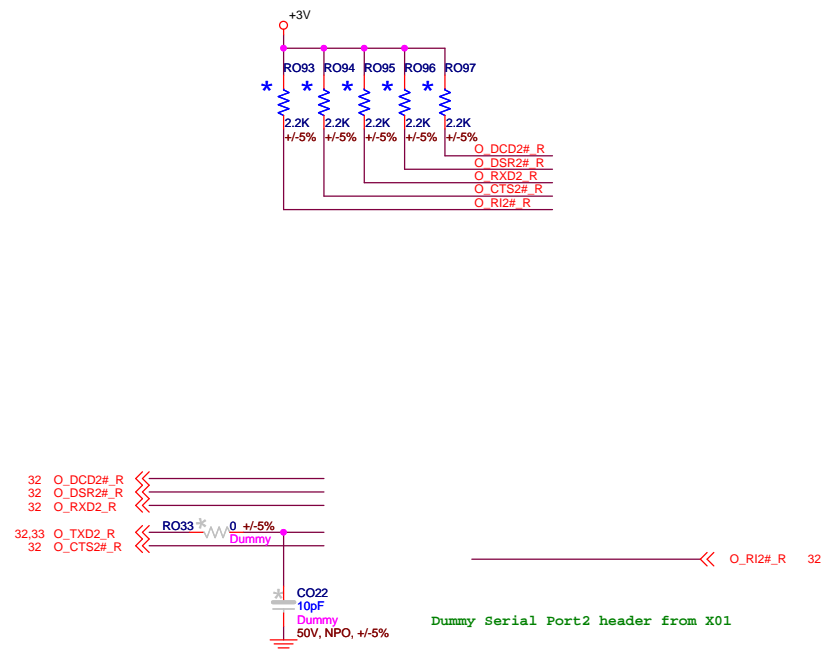


INC.

Title		
EMI		
DWG NO	Lanikai_MT/DT	Rev
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Move PWR_SW conn to
page56 20091126

Serial Port 2 Header



Title		
COM2 HDR		
DWG NO	Rev	
Lanikai_MT/DT	A00	
Date:	Sheet	of
Wednesday, June 13, 2012	55	71

Front USB/LED Header

Pitch 2.0mm

+3V

RNO2 8.2KOhm +/-5%

O_FIO_SATA_LED#

T_SATALED#

OQ14_C

S_FP_CHAS_DET#

22 U_USB10N >> RU38 0 Dummy U_USB10N_R

22 U_USB10P >> RU39 0 Dummy U_USB10P_R

22 U_USB11N >> RU41 0 Dummy U_USB11N_R

22 U_USB11P >> RU42 0 Dummy U_USB11P_R

20110212 Change to 2x13 for Front USB x2 port.

20110212 Change to 2x13 for Front USB x2 port.

MT/DT CHASSIS

FP_CHAS_DET#	MT/DT
0	MT
1	DT

POWER SWITCH Header

U_USB11N_R 1 UU5 6 U_USB11P_R

U_USB10N_R 2 5 USBPWR7_F_50

U_USB10P_R 3 4 U_USB10P_R

IP4220C26

U_USB10P_R 1 LU11 4 >> U_USB10P 22

U_USB10N_R 2 3 >> U_USB10N 22

Common Choke 90 Ohm

U_USB11N_R 2 LU12 3 >> U_USB11N 22

U_USB11P_R 1 4 >> U_USB11P 22

Common Choke 90 Ohm

5VSB

RO34 499 +/-1%

RO67 100 +/-5%

PWR_SW

Header_2X3_K5

5VSB

RO37 499 +/-1%

O_FP_CBL_DET# 32

O_YELLOW# 32

O_PWRBTN#IN

O_GREEN#

O_FP_CBL_DET#

RO70 8.2K +/-5%

3V_DUAL

CO27 470pF

CO54 470pF Dummy

CO52 470pF Dummy

50V_X7R +/-10%

50V_X7R +/-10%

50V_X7R +/-10%

O_FIO_SATA_LED#

CO53 470pF Dummy

50V_X7R +/-10%

5VSB

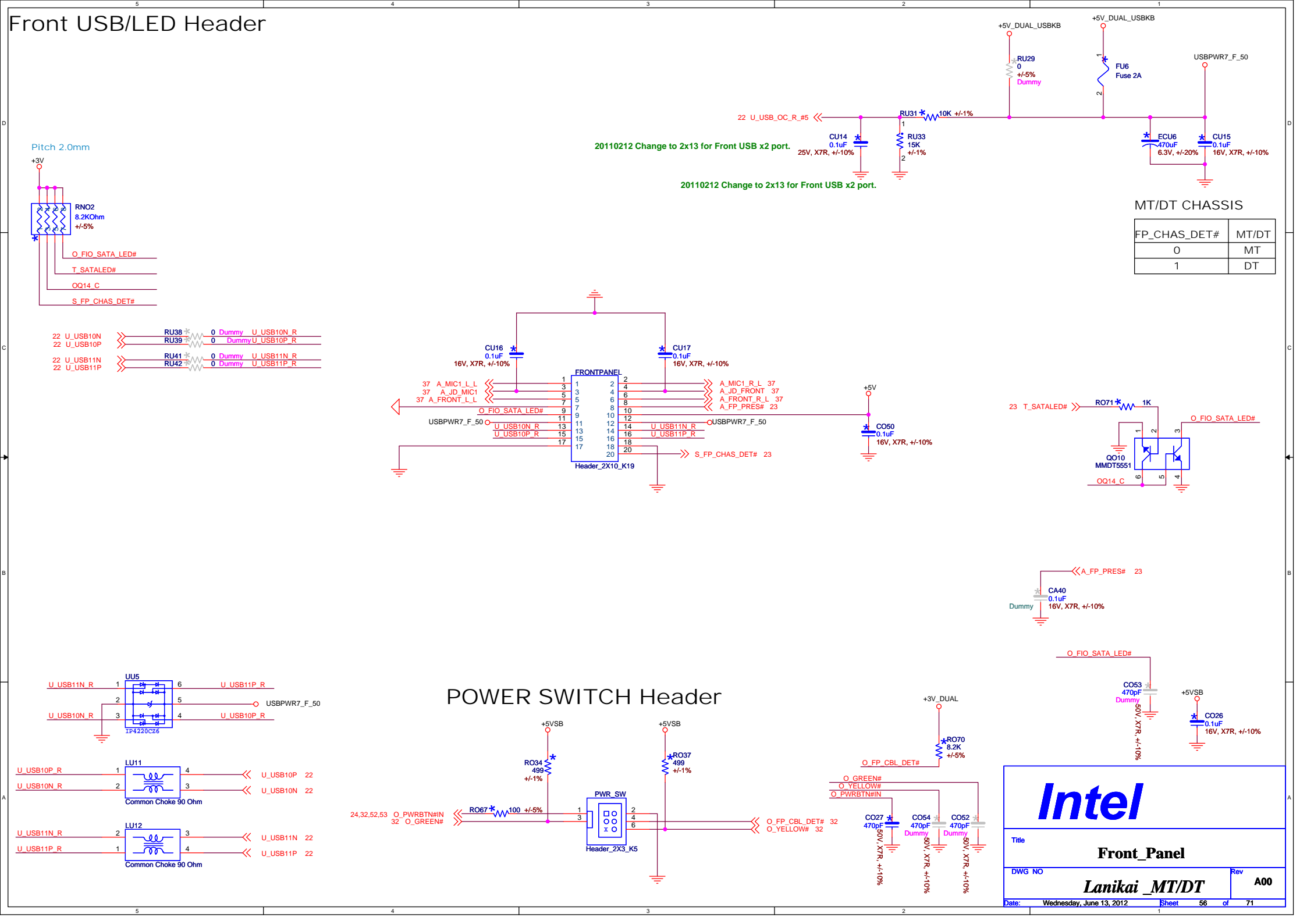
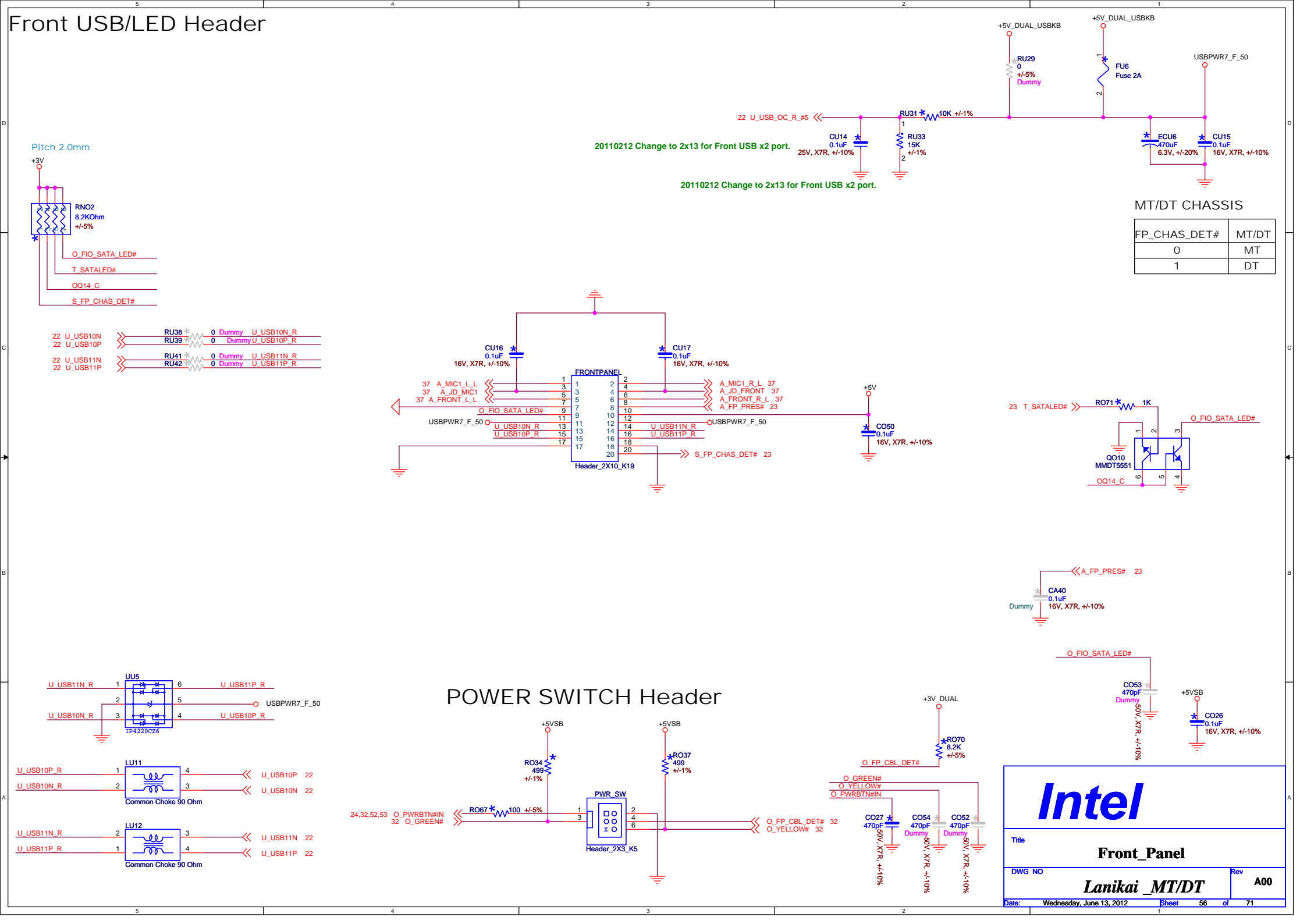
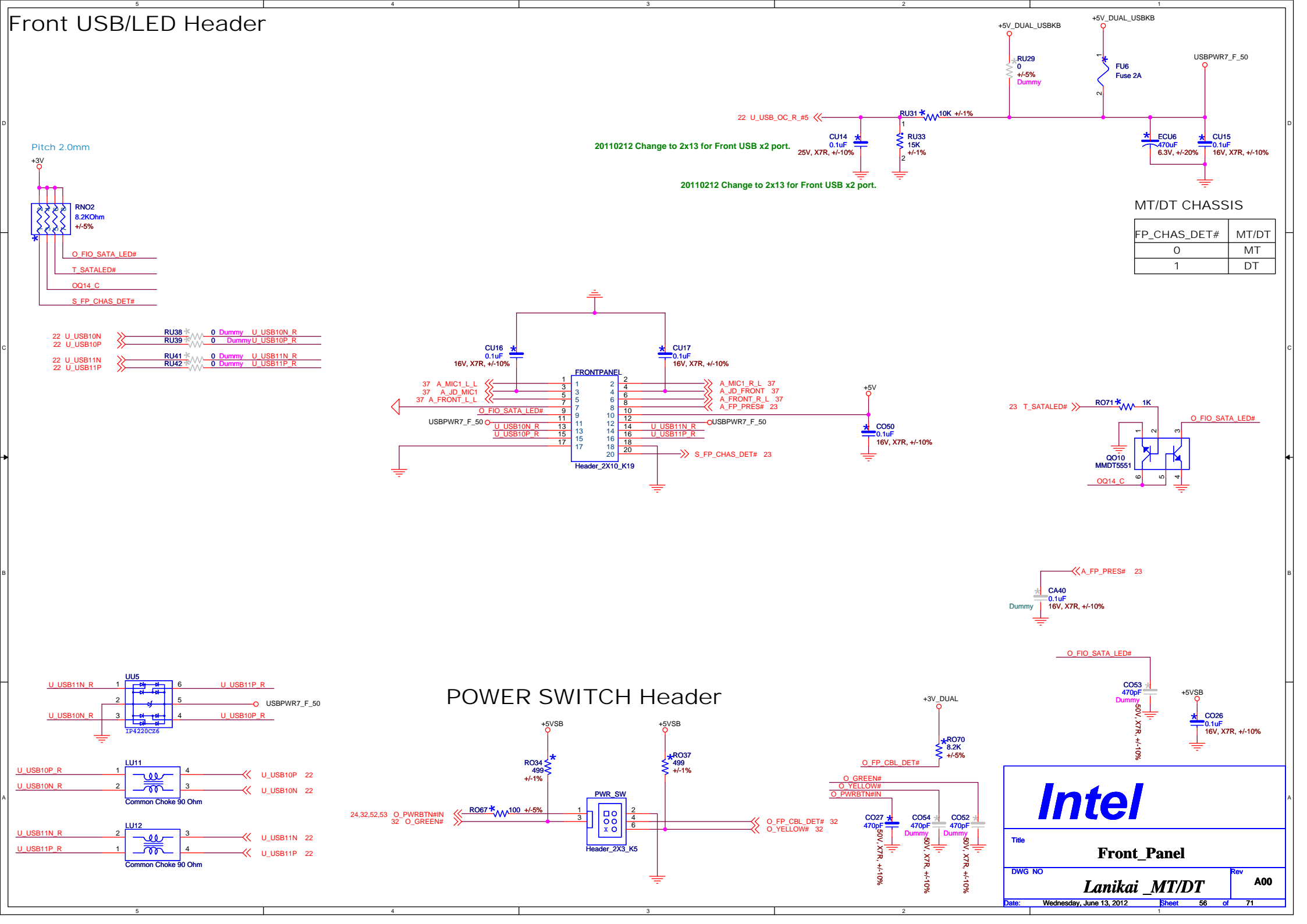
CO26 0.1uF 16V, X7R, +/-10%

Intel

Front_Panel

DWG NO **Lanikai_MT/DT** Rev **A00**

Date: Wednesday, June 13, 2012 Sheet 56 of 71

[illegible][illegible][illegible]

Front USB/LED Header

Pitch 2.0mm

+3V

RNO2 8.2KOhm +/-5%

O_FIO_SATA_LED#

T_SATALED#

OQ14_C

S_FP_CHAS_DET#

22 U_USB10N >> RU38 0 Dummy U_USB10N_R

22 U_USB10P >> RU39 0 Dummy U_USB10P_R

22 U_USB11N >> RU41 0 Dummy U_USB11N_R

22 U_USB11P >> RU42 0 Dummy U_USB11P_R

20110212 Change to 2x13 for Front USB x2 port.

20110212 Change to 2x13 for Front USB x2 port.

MT/DT CHASSIS

FP_CHAS_DET#	MT/DT
0	MT
1	DT

POWER SWITCH Header

U_USB11N_R 1 UU5 6 U_USB11P_R

U_USB10N_R 2 5 USBPWR7_F_50

U_USB10P_R 3 4 U_USB10P_R

IP4220C26

U_USB10P_R 1 LU11 4 >> U_USB10P 22

U_USB10N_R 2 3 >> U_USB10N 22

Common Choke 90 Ohm

U_USB11N_R 2 LU12 3 >> U_USB11N 22

U_USB11P_R 1 4 >> U_USB11P 22

Common Choke 90 Ohm

5VSB

RO34 499 +/-1%

RO37 499 +/-1%

RO67 100 +/-5%

24,32,52,53 O_PWRBTN#IN 32 O_GREEN#

O_FIO_SATA_LED#

O_GREEN#

O_YELLOW#

O_PWRBTN#IN

O_FP_CBL_DET# 32

O_YELLOW# 32

3V_DUAL

RO70 8.2K +/-5%

CO27 470pF

CO54 470pF Dummy

CO52 470pF Dummy

CO26 0.1uF 16V, X7R, +/-10%

CO53 470pF

5VSB

CA40 0.1uF 16V, X7R, +/-10%

O_FIO_SATA_LED#

CO53 470pF

5VSB

CO26 0.1uF 16V, X7R, +/-10%

Intel

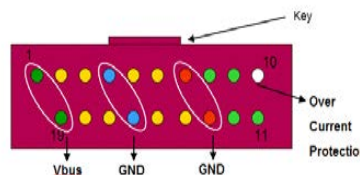
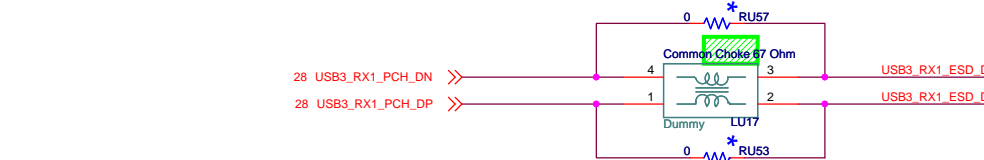
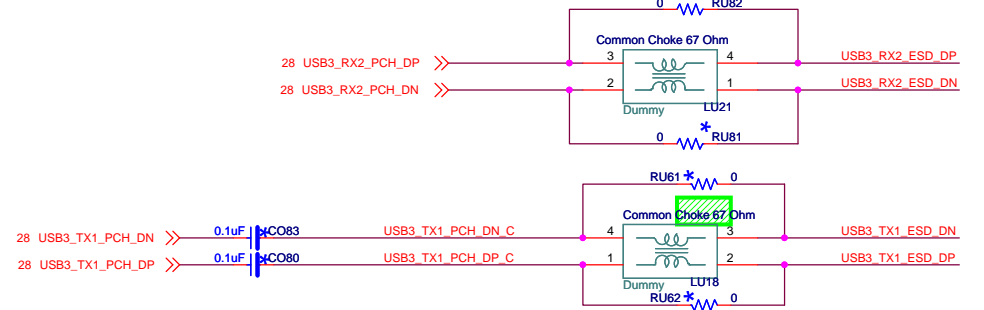
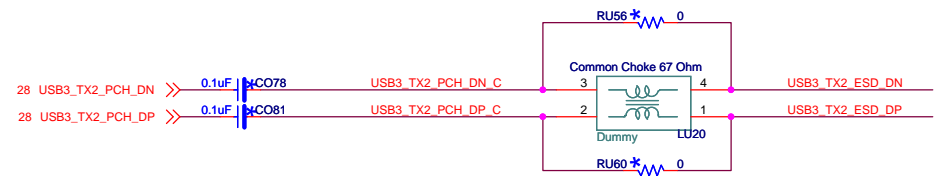
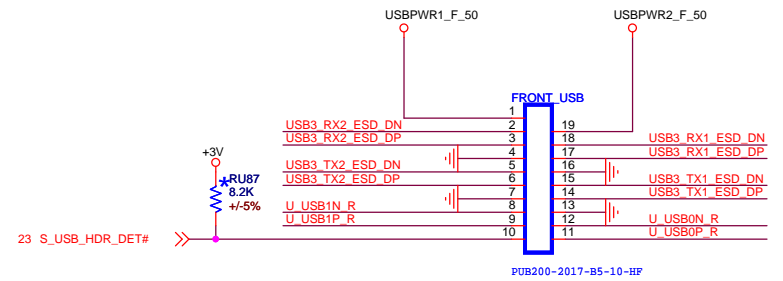
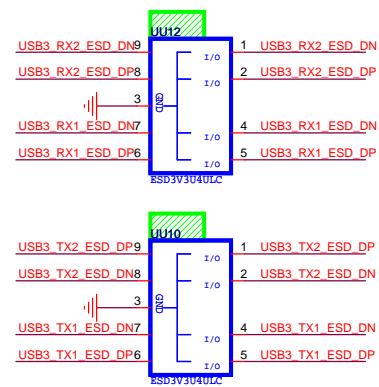
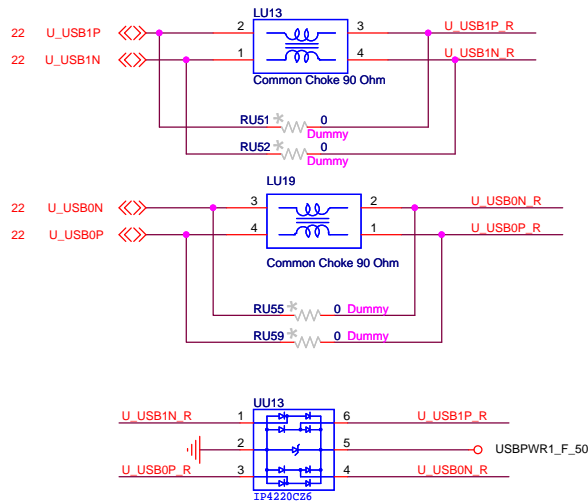
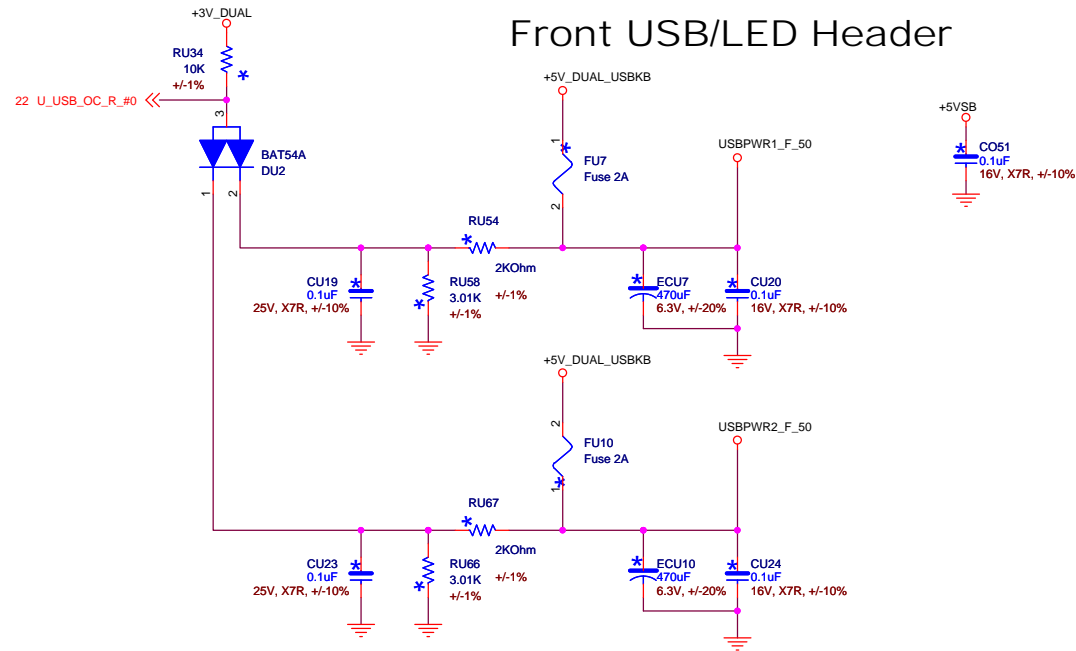
Front_Panel

DWG NO **Lanikai MT/DT** Rev **A00**

Date: Wednesday, June 13, 2012 Sheet 56 of 71

[illegible]

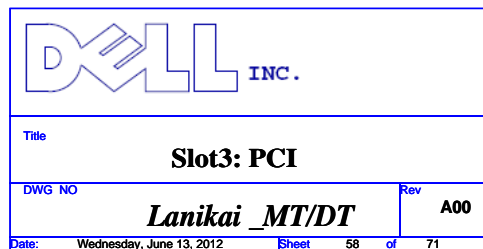
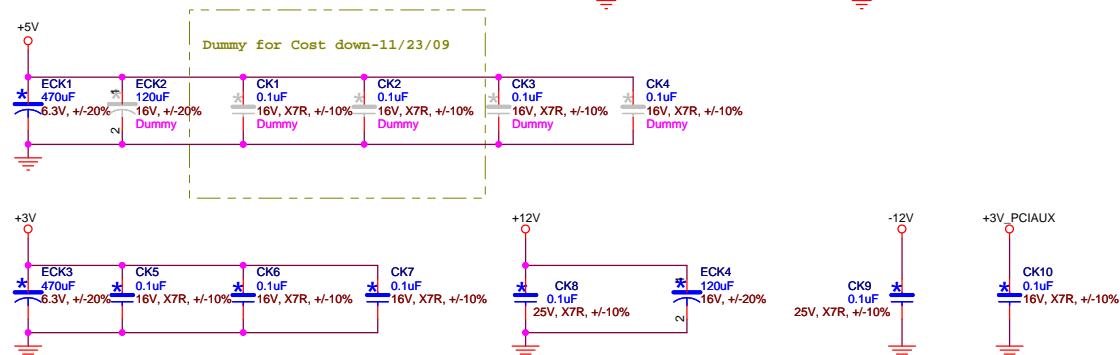
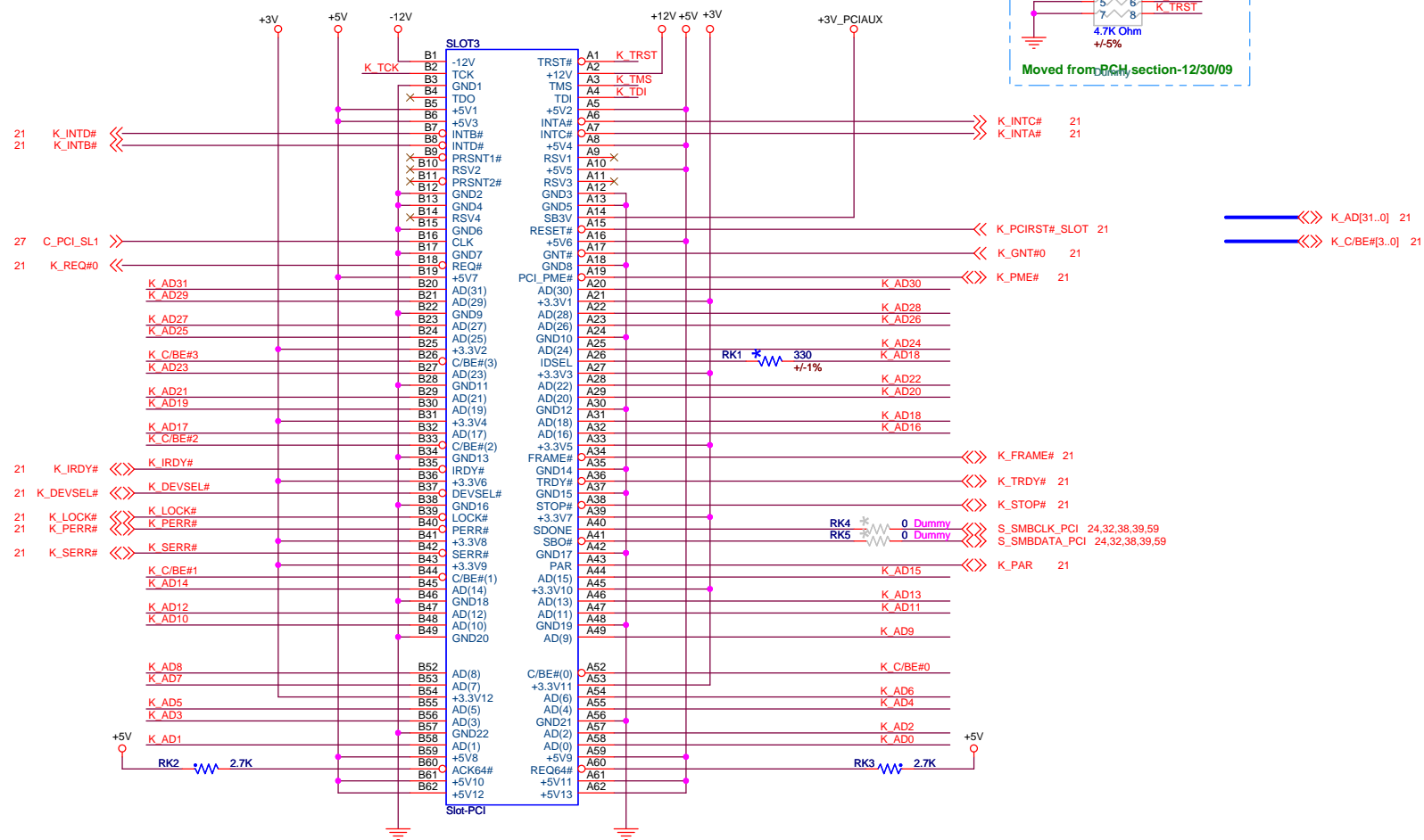
Front USB/LED Header

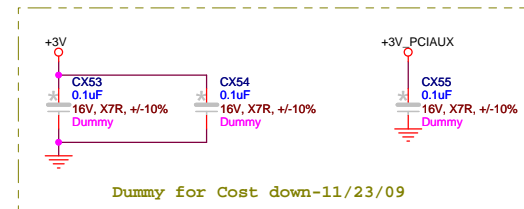
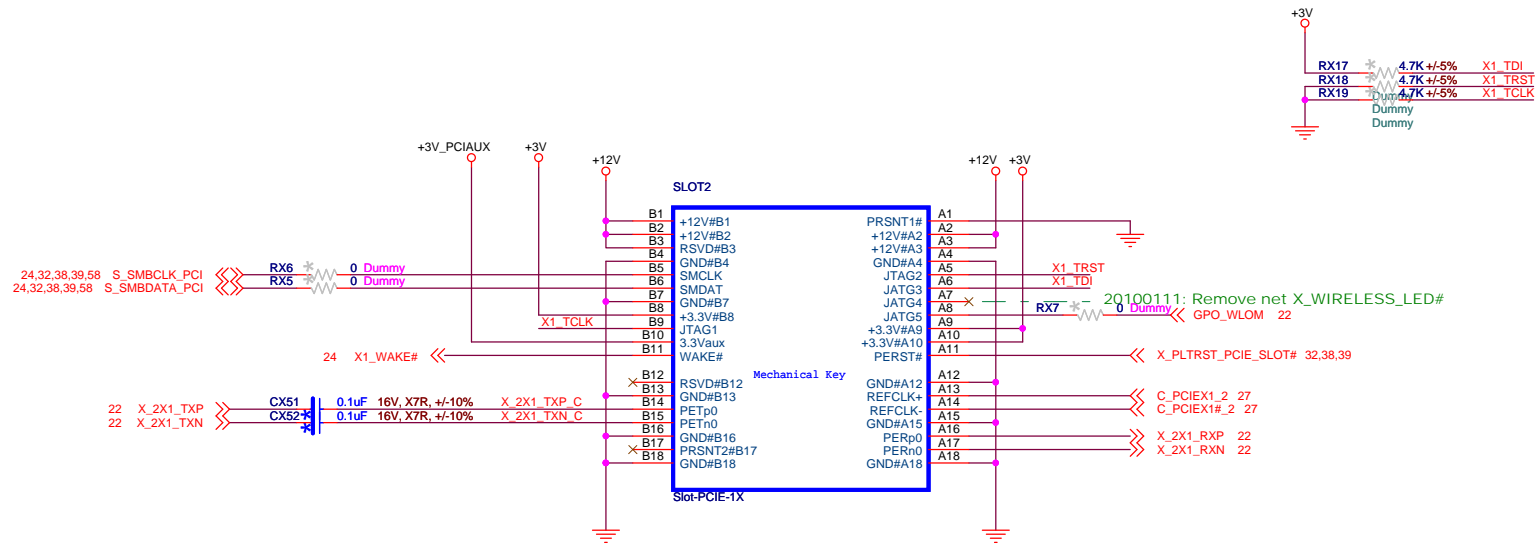


Intel

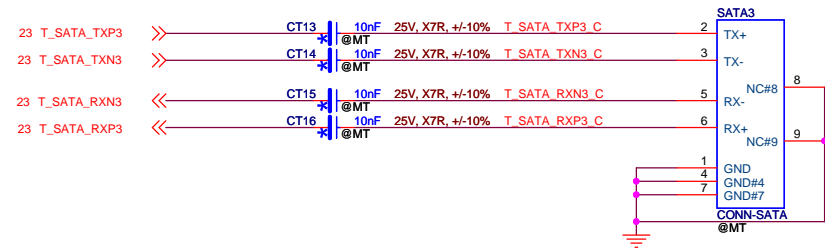
Title		TBD	
DWG NO	Lanikai_MT/DT		Rev A00
Date:	Wednesday, June 13, 2012	Sheet	57 of 71


IRQ: CDAB
IDSEL: AD18
REQ/GNT: 0





SATA port 3 only for MT



 **INC.**

Title

SATA_MT

DWG NO

Lanikai_MT/DT

Rev

A00

Date:

Wednesday, June 13, 2012

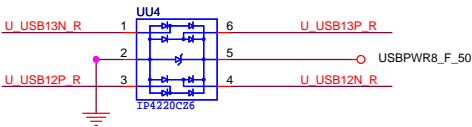
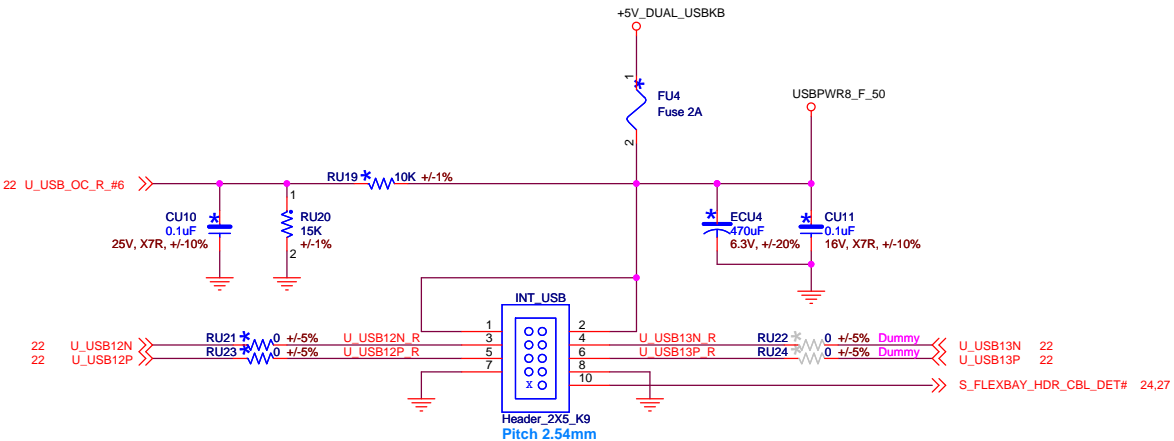
Sheet

60

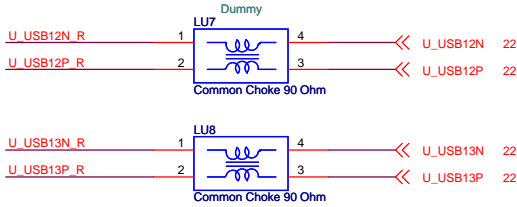
of

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FLEXBAY



stuff on 20100723-EMC request



CO-LAY with 4 Serial resistors RU21, RU22, RU23, & RU24



Title

Flexbay USB_MT

DWG NO

Lanikai_MT/DT

Rev

A00

Date:

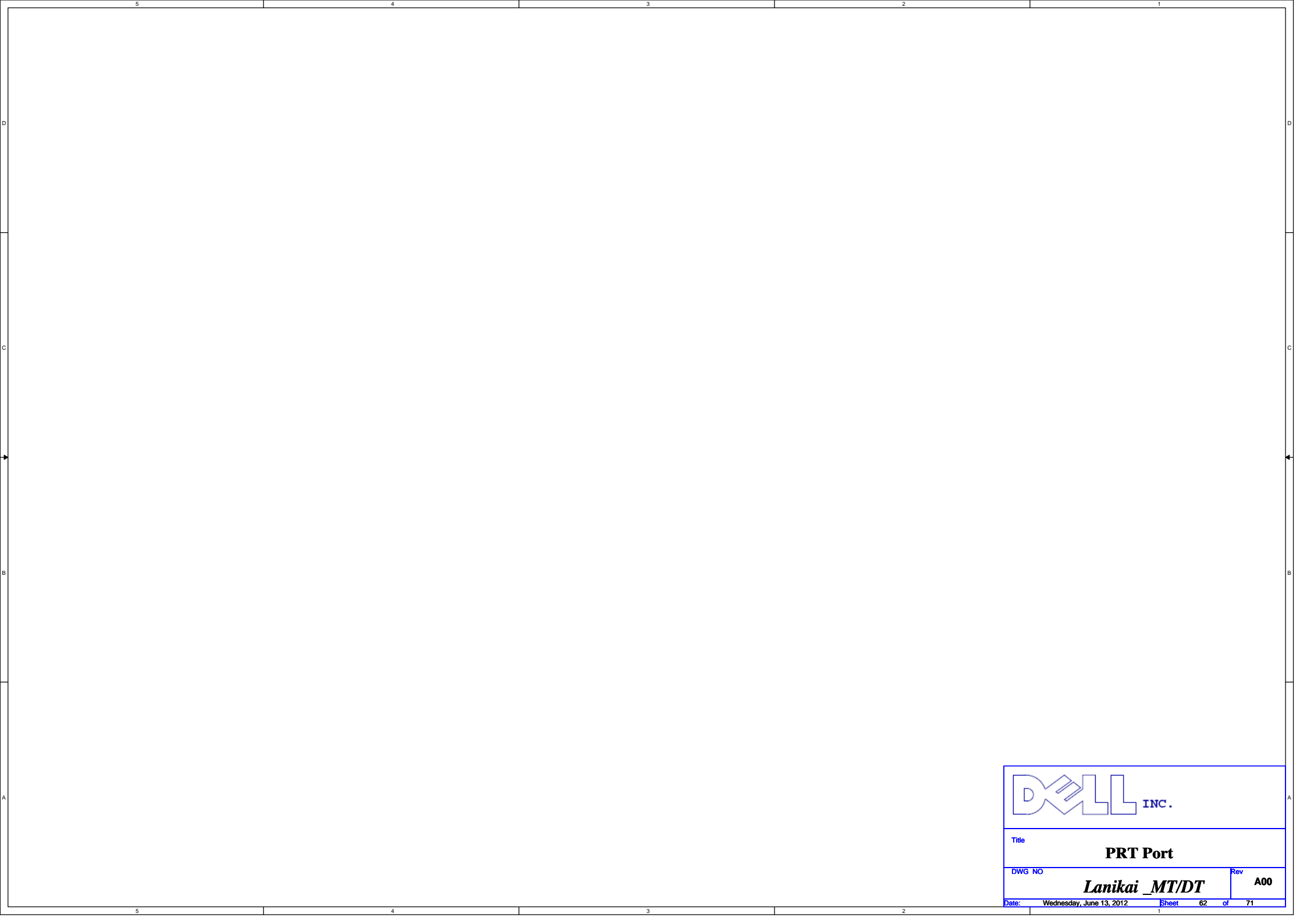
Wednesday, June 13, 2012


Sheet

61

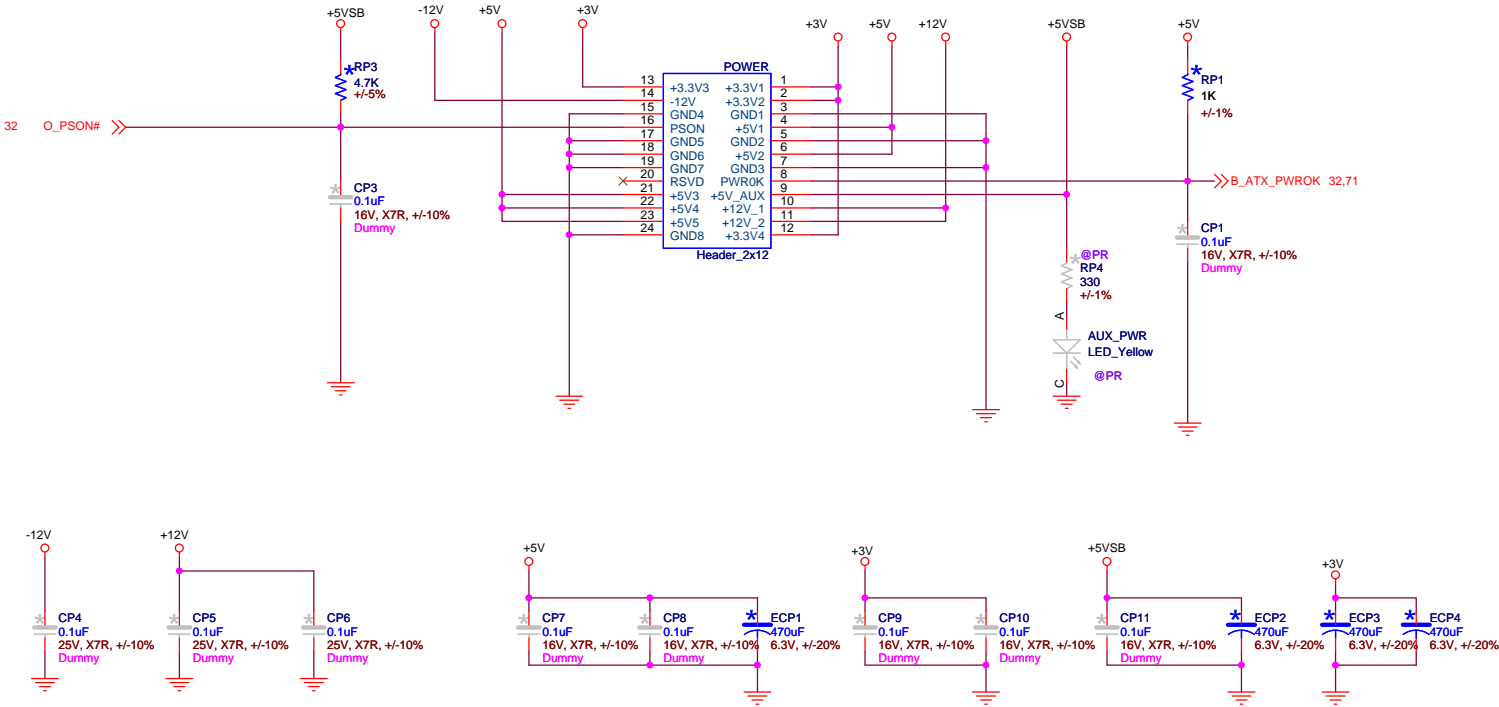
of

71



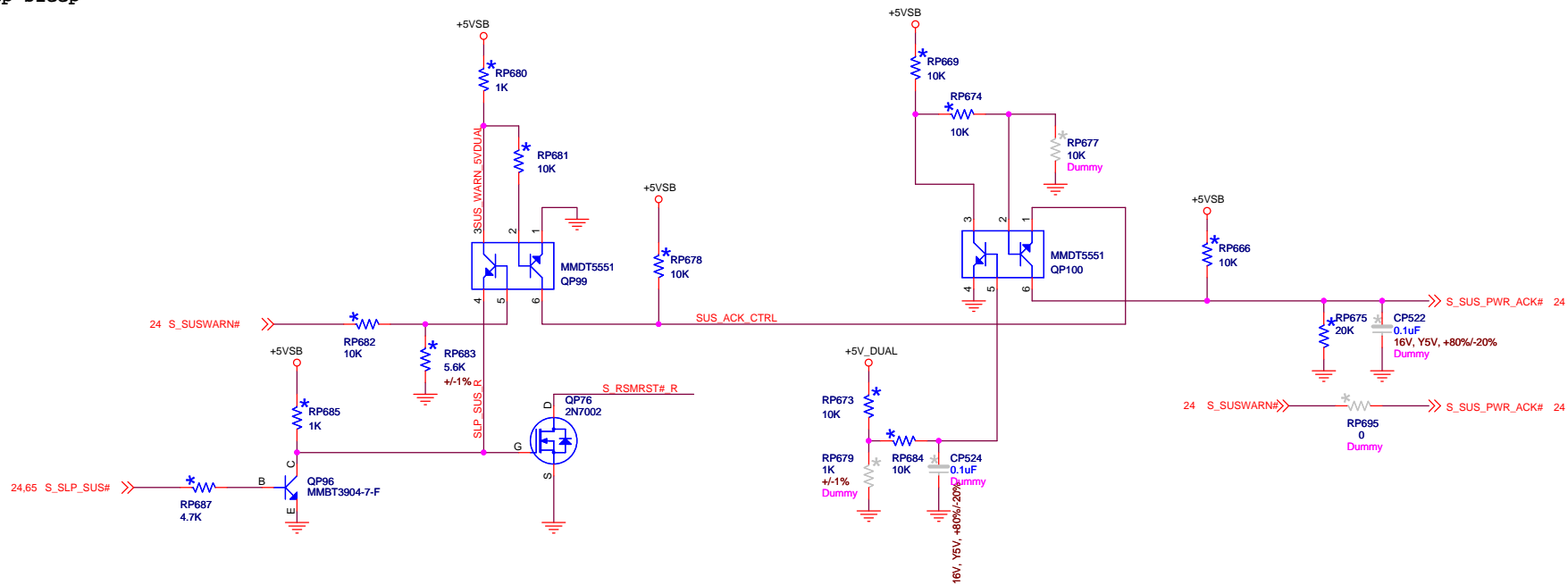
 INC.			
Title PRT Port			
DWG NO		Rev A00	
Date: Wednesday, June 13, 2012		Sheet 62 of 71	

ATX POWER CONNECTOR

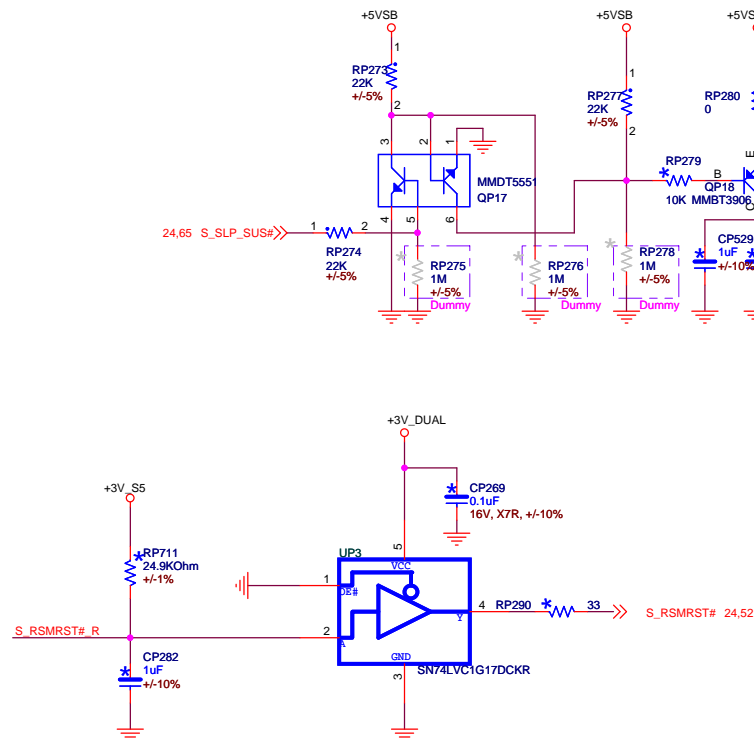


Title			Power Conn		
DWG NO			Lanikai_MT/DT		
Date: Wednesday, June 13, 2012			Sheet 63 of 71		
			Rev A00		

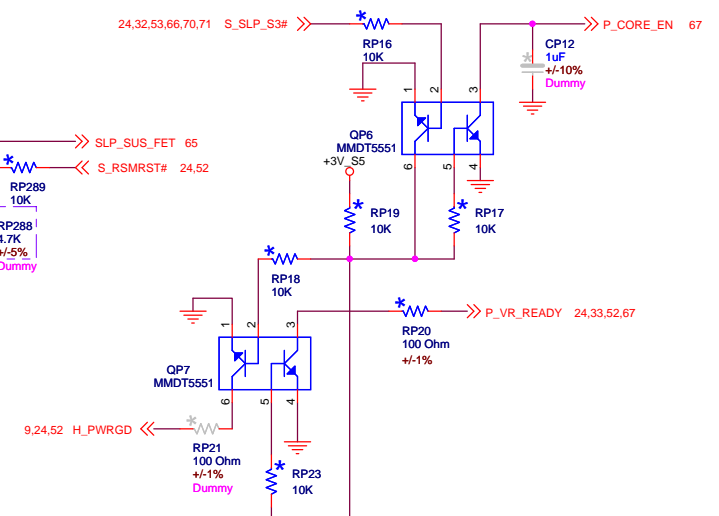
For Deep Sleep



RESUME RESET Logic

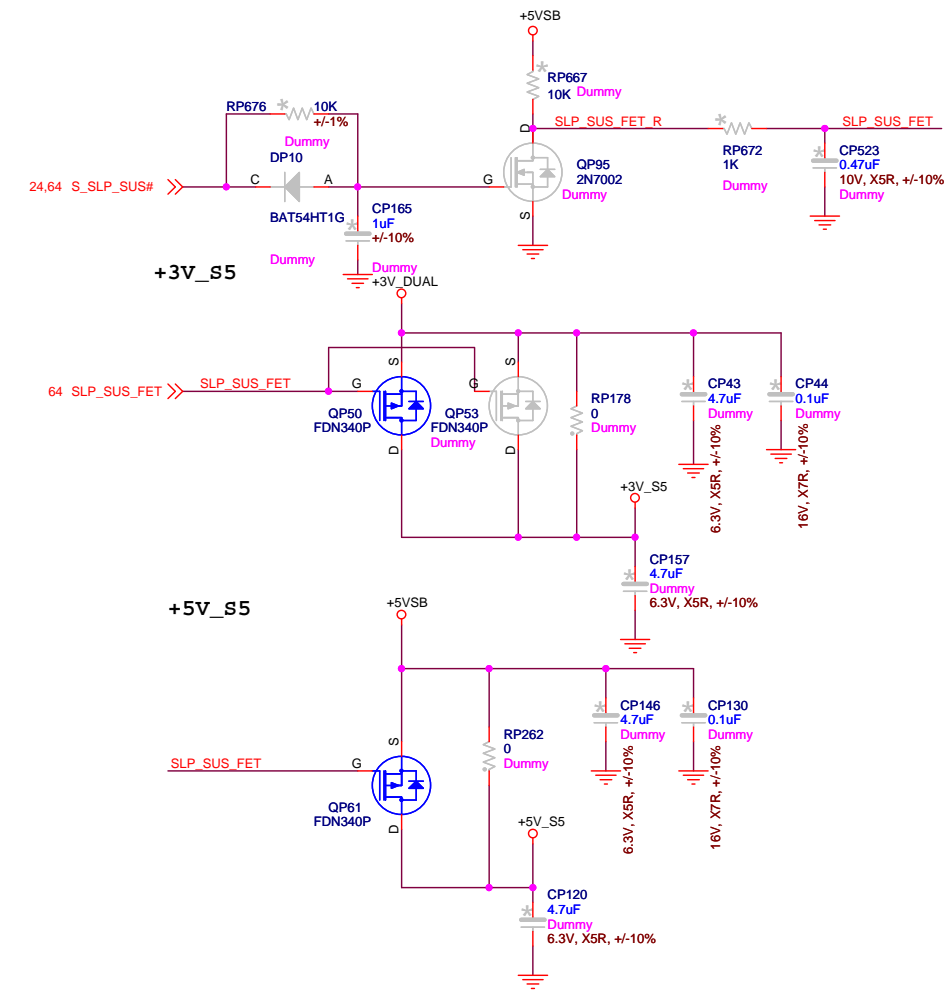
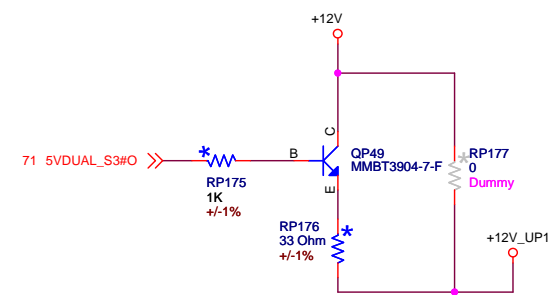
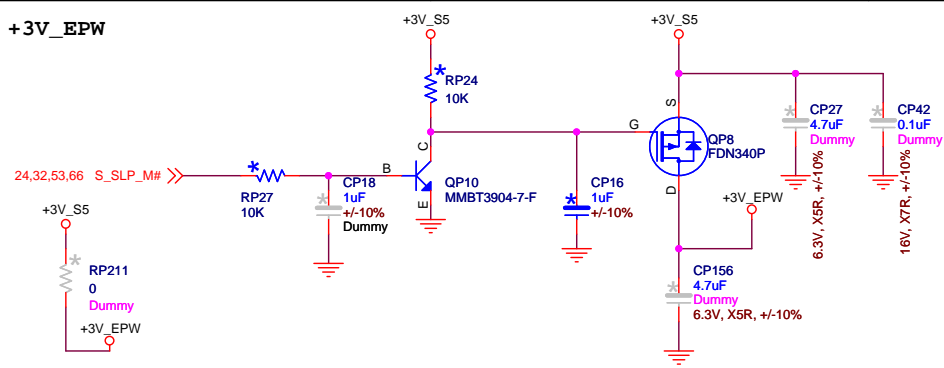


VR_READY DEFENSIVE

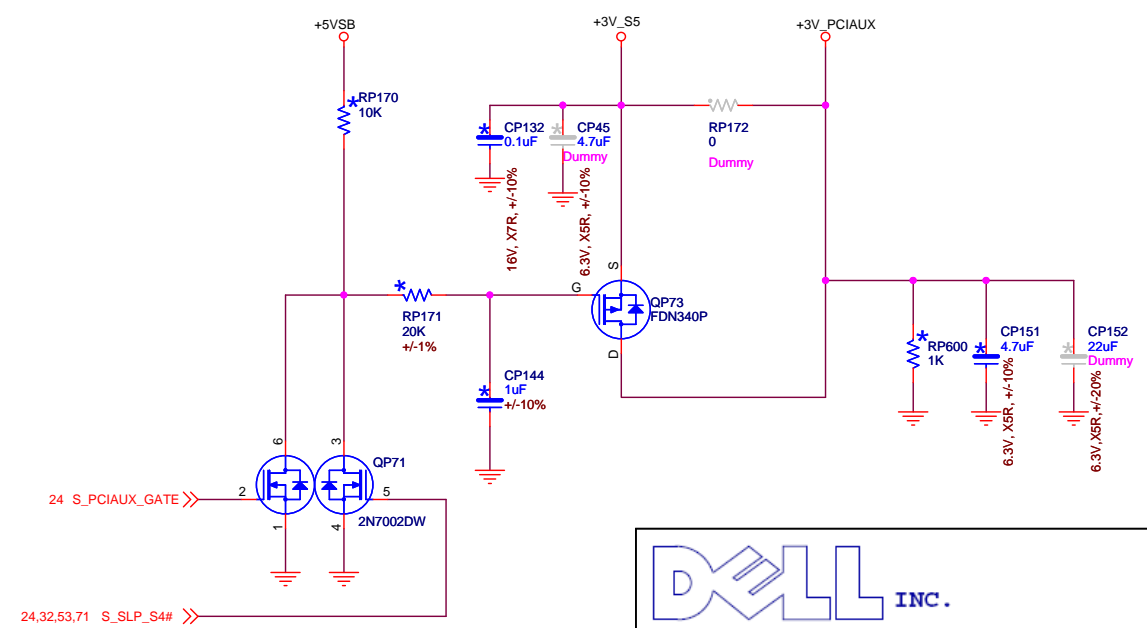


Title		
Power Sequence		
DWG NO	Lanikai_MT/DT	Rev A00
Date: Wednesday, June 13, 2012	Sheet 64	of 71

+3V_EPW

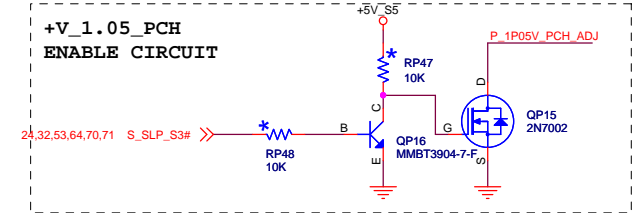
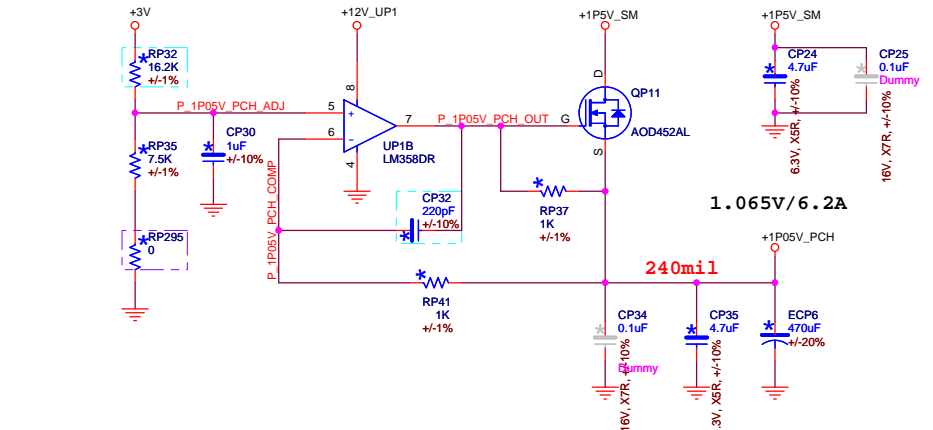


+3V_PCIAUX(FOR PCI/PCIE SLOT)

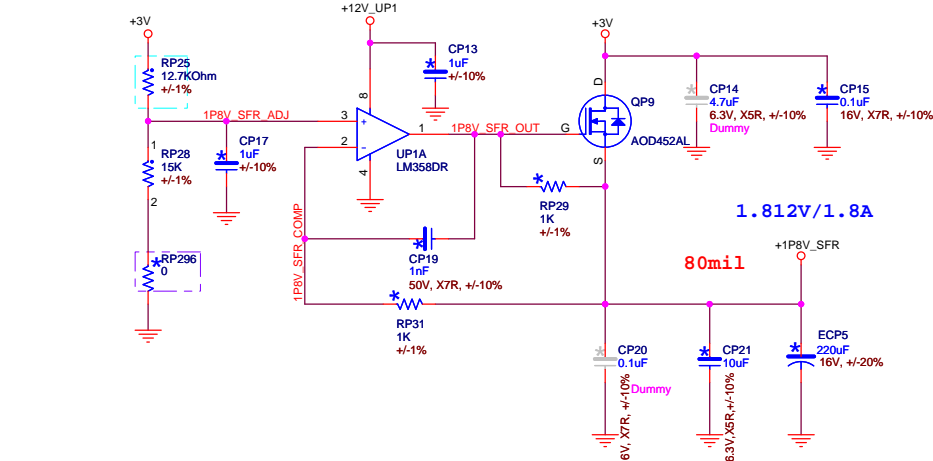


Title		Power-1:Linear Power-1	
DWG NO		Lanikai_MT/DT	
Date: Wednesday, June 13, 2012		Sheet	65 of 71

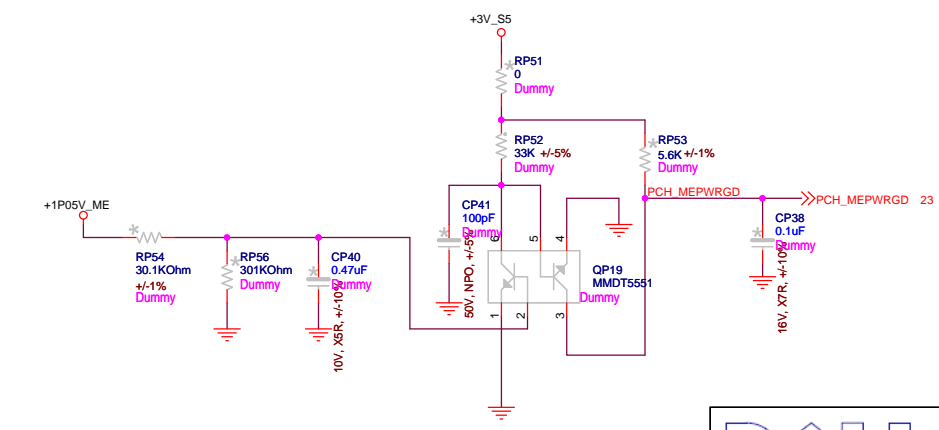
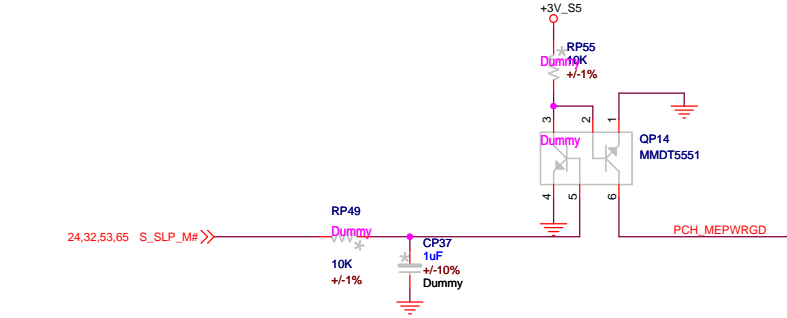
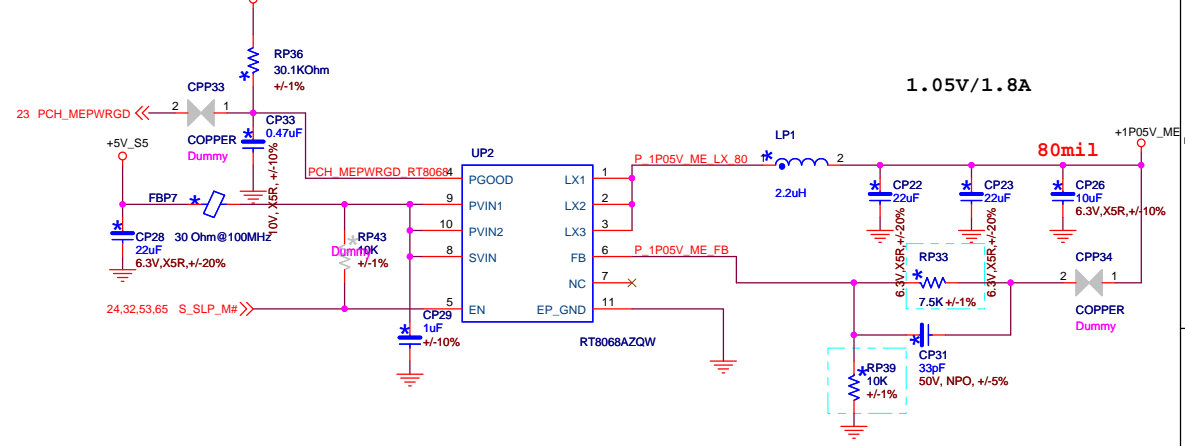
+V_1.05_PCH



+V_1P8_SFR

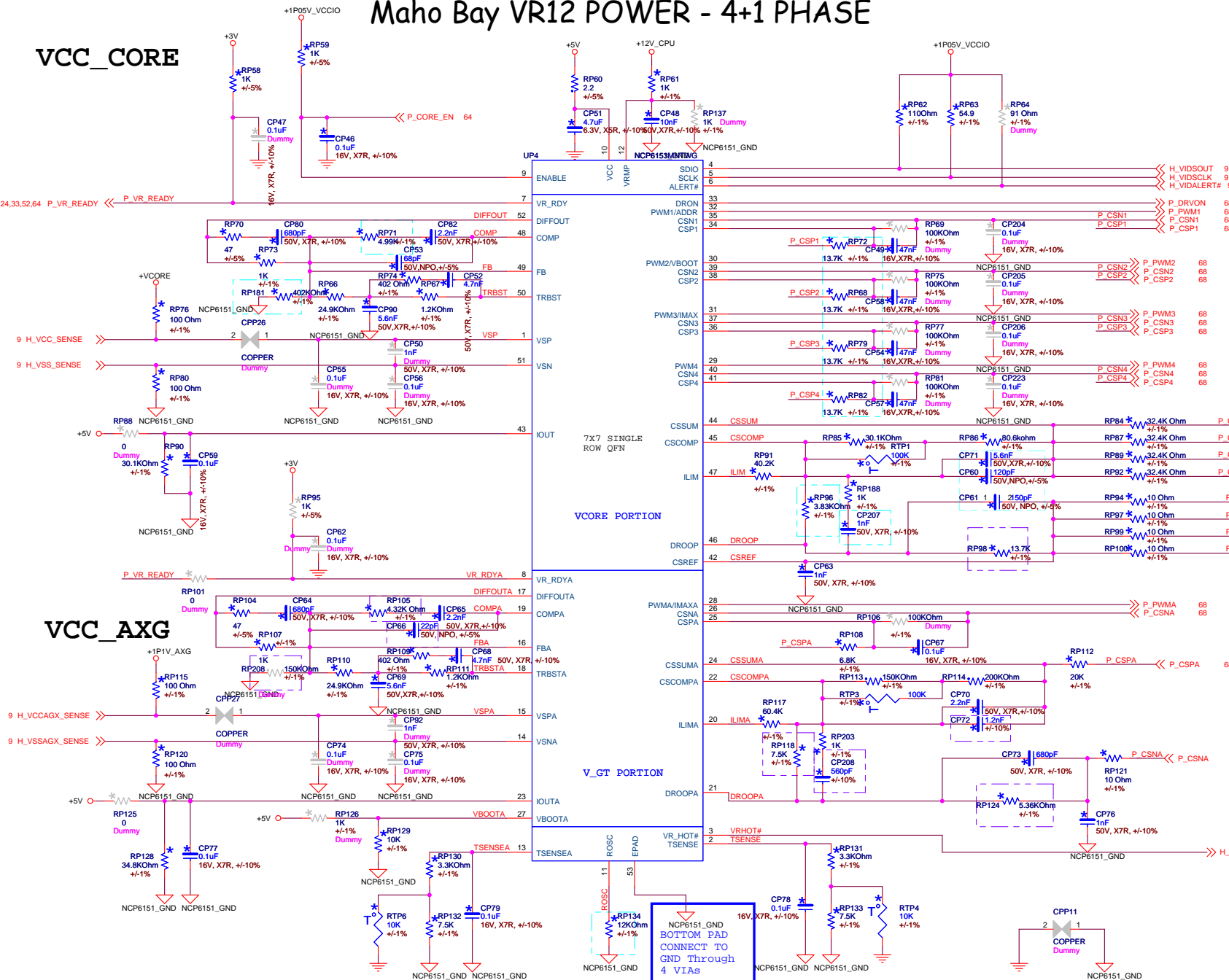


+V_1.05_ME



Maho Bay VR12 POWER - 4+1 PHASE

VCC_CORE



PWM ADDRESS

RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE

RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1.0V
70K	1.1V
95K	1.2V
135K	1.35V
165K	1.5V

